Understanding and Optimization of Electrical Characteristics of Organic Devices

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by

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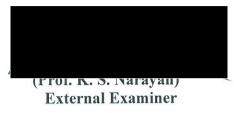
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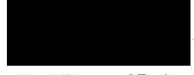
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Abstract

The electrical characteristics of organic semiconductors have been studied intensively ever since conductivity in organic materials has been discovered. The focus has been the understanding of factors that affect charge transport so that the performance of organic devices can be improved. This work focuses on the electrical characterization of organic semiconductors. We have investigated a series of problems related to capacitance voltage measurements and current voltage measurements of organic devices.

The physics of organic electronic devices are often interpreted by invoking the concept of "unintentional doping." However, the applicability and usefulness of this controversial concept is not very clear and is under much debate, recently. In this thesis, we have reevaluated the validity of this concept through careful experiments and detailed numerical simulations. Specifically, we have used Capacitance Voltage (CV) measurements of pentacene devices as a test bed to unravel the role of injecting electrodes and unintentional doping (if any). Our results have indicated that the CV of pentacene capacitors can be solely understood in terms of properties of the contact electrodes. The unintentional doping, if present, has an inconsequential role in device performance. Our conclusions have indicated that, often, an incorrect interpretation of CV results leads to unphysical values of unintentional doping. It has obvious implications in the fundamental understanding of organic semiconductor device physics, modeling, and characterization thus resolving many ambiguities in literature by providing a consistent interpretation through a coherent conceptual framework.

The impact of atmospheric exposure on pentacene devices has been explained based on the contact barrier degradation at the metal-semiconductor interface. An analytical model based on the timing analysis of the capacitance frequency measurements has been proposed in order to extract the injection barrier. It was found that on atmospheric exposure, the pentacene gold injection barrier is reduced to 0.51 eV limiting the number of carriers transporting in the devices. The extracted value is close to different values reported in various photoelectron spectroscopic studies.

Mechanical flexibility is one of the key advantages of organic semiconducting films in applications such as wearable-electronics or flexible displays. We have studied the electrical characteristics of C_{60} -based top gate organic field effect transistors (OFET). The devices were characterized by curling the substrates in a concave and convex manner, to apply varying values of compressive and tensile strain, respectively. Electron mobility was found to increase with compressive strain and decrease with tensile strain. The observed strain effect was found to be strongly anisotropic with respect to the direction of the current flow. The results are quantified using the Fishchuk/Kadashchuk model for the hopping charge transport. We suggest that the observed strain dependence of the electron transport is dominated by a change in the effective charge hopping distance over the grain boundaries in polycrystalline C_{60} films.

Most studies on charge transport are focused around low temperature electrical measurements. We have electrically characterized pentacene based OFETs between the temperature ranges of 25 °C to 190 °C in ambient conditions. Material characterization studies such as X-ray photoelectron (XPS), X-ray diffraction (XRD) and atomic force microscopy (AFM) prove the stability of pentacene as a semiconductor in ambient conditions at elevated temperatures. The crystallinity of pentacene films is retained up to 110 °C; its phase changes around 150 °C. Charge transport studies reveal a strong dependence of mobility on the gate field and interface states. The degradation of device parameters is attributed to the deterioration of dielectric and phase transformation in pentacene at higher temperatures. At an above-room-temperature range, mobility is found to be thermally activated in the presence of traps, whereas, for a trap-free interface, it is temperature-independent. These results validate the performance and stability of organic devices in practical environmental conditions.

The different experimental works reported in this thesis have been wrapped under the thesis title, "Understanding and Optimization of Electrical Characteristics of Organic Devices".

Keywords: Capacitance Voltage, Current Voltage, Mobility, Injection Barrier, C60, Pentacene, Stability, Reliability, Strain, High Temperature.

Acknowledgement

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In the past five years, I have had the opportunity to learn some very exciting things, meet intelligent people, and make some great friends. There is long list of people whom I wish to thank for their support during the thick and thin of these years.

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During the tenure of Ph.D programme, I did an internship at Johannes Kepler University (JKU) for four months. The discussion with Guenther, Mujeeb and guidance by Clemens and Prof. Sitter helped in improving the quality of organic transistors fabricated at IIT Bombay. It was the involvement of Prof. Pradeep Nair that made me realize the importance of simulations in my work. The meticulous guidance by him added a new dimension to my learning curve in both aspects technical and non-technical. Toward the final year of my Ph.D tenure, I got the opportunity to interact with Prof. Narasimhan and Prof. Kabra; their guidance helped me diversify my knowledge of the field and complete the final steps of my research. In addition, I am indebted to all the faculties of IITBNF, in whose office, I use to drop unannounced they have been kind enough to entertain my queries. Experimental work requires lot of external support; all the credit for 24x7 support goes to the dedicated staff at IITBNF. Arvind, Pradeep, Sunil, Bhimraj, Vinayak and others who have worked relentlessly to help me in debugging the experimental setup deserve recognition for their efforts. The administrative staff of IITBNF also has been supportive in the purchase and procurement of consumables. Arthi madam, Kuldeep Patil, and others have always gone out of their way to support us.

I am a collaborative student of a joint venture between IIT Bombay and Monash University. I would like to acknowledge the efforts of our management unit at IITB-Monash Research Academy who have done a great job in synchronizing the protocols at the two institutes and simplifying academic processes for us. Our AECs and other staff at Academy have actively guided us with all the paper work. Inputs from Prof. Mohan Krishnmoorthy along with other Academy activities like the 3MTT, and the communication workshops have helped me in improvising my presentation skills.

A journey becomes an adventure with the right company. I have been fortunate enough to be blessed with a perfect set of friends and colleagues who have made these five years nothing less than an adventure. The constructive criticism and motivation by friends such as Abhishek Misra, Harshil Raval, Kaustaubh Joshi, Subhadeep Mukhopadhyay, Prashant Pramahans, Raju, Pankaj Kumbhare, Ravikesh, Edmund Caravalho, Saumya Nigam, Jasvipul Chawala, Pranab Mohopatra, Dushyant Kushwaha, Tarun Garg and many others have kept me afloat during the lean phases. It was at events such as the fluid seminar where most of the philosophical learning has happened. I must also acknowledge my bike and friends from cycling community for the many adventures we went on whenever I needed a break.

Finally, I express my gratitude to Ma, Papa and Bhai for their constant faith in me.

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Chapter 1.

Introduction

The aim of this chapter is to provide the background for the research done in this thesis. A brief history of the development and the state-of-art of organic electronics has been presented. The problem statement for this thesis has been formulated and the thesis outline describes the details of the work done towards for the completion of the Ph.D degree.

1.1. Historical Background

The developments in human pursuits in the last four decades can easily be associated with the evolution of the world of electronics. It was in 1948 that the first Transistor was fabricated in Bell Lab by John Bardeen, Walter Brattain and William Shockley. They were jointly awarded the Nobel Prize in physics in 1956. It eventually led to the fabrication of the Bipolar Junction Transistor (BJT) which is still very useful in analog designs. The next major breakthrough came in 1960 in the form of the Metal-Oxide-Semiconductor (MOS) Transistor. A Field Effect Transistor (FET) was fabricated in Bell labs by John Atalla and Dawon Kahng based on a design patented around 60 years ago by Julius E. Lilienfeld. An MOS transistor is a three-terminal device with the gate separated from the semiconductor by an insulator and the current between the source and drain controlled by the gate voltage. MOS technology is one of the key technologies present today and the devices discussed in this thesis are based on the MOS concept.

Most of the present generation electronic devices are fabricated out of inorganic semiconductors such as silicon and germanium. Over the years, performance enhancement has led to the scaling of MOS devices. In present times, source drain distance has come down to tens of nanometers, reaching the limits of interatomic distance. It will not be long when the growth of silicon industry will come to a halt due to practical limitations. Academia and the industry have started exploring alternative growth models based on different types of semiconductors.

1.2. Organic Electronics: Introduction

Plastics are pervasive in modern life. Ever since its discovery in 1800, the importance of plastic has been established in our lives in the form of household appliances, electrical appliances and various other forms of basic utilities. Plastic is cheaper, lighter compared to metals and can easily be molded into different shapes. Plastic was commonly known to be an insulator until 1963 when Weiss et al. reported high electrical conductivity in iodine-"doped" oxidized polypyrrole [1]. However, the discovery was largely overlooked until high conductivity in doped polyacetylene was discovered in 1977 by Heeger et al.[2]. It attracted the attention of the researchers from different field and the growth story of conducting organic

materials started. As a result in the year 2000, the Nobel Prize was jointly awarded to Prof. Alan J. Heeger, Prof. Alan G. MacDiarmid and Prof. H. Shirakawa for their pioneering work on conducting organic polymers [3]. The possibility of combining the properties of plastics (low cost, flexibility, low temperature processing) with the tunable electrical properties of organic materials (metallic, semiconducting and insulating) opened up a new window of possibilities for research and applications in the field, referred to as Organic Electronics (OE).

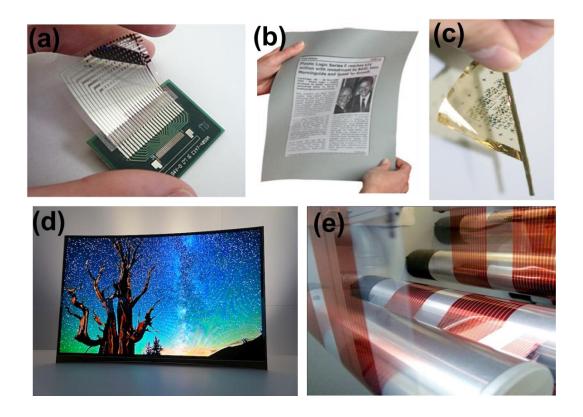


Figure 1.1 Different examples of organic electronics devices (a) Flexible 16-byte organic non-volatile bistable memory demonstrated at the 2007 IEEE International Electron Devices Meeting by the researchers from National Chung Hsing University and Industrial Technology Research Institute, Taiwan[4] (b) Plastic Logic demonstrated an organic active matrix display driving electronic paper at the 12th International Display Workshop in Takamatsu, Japan, on December 7, 2005. (c) Ultra Flexible circuits fabricated on 12.5 μ m substrate with a bending radius of 100 μ m [5] (d) Curved OLED TV demonstrated in international markets (e) Roll-to-roll printing of organic circuits [6]

Organic Electronics presents a new dimension to the conventional form of electronics that we have known so far as being expensive, brittle, requiring high temperature processing, and giving low throughput. The world of Organic Electronics (OE) paves the way for the flexible electronics made of Organic Semiconductors (OSC). OE offers an advantage over conventional electronics in the form of low cost of fabrication, room temperature processing, being light weight, having flexibility, having a large area and high throughput. The niche areas of application for OE are flexible display, RFiD tags, E-paper, implantable medical devices, large sensor arrays, electronic textiles etc. Figure 1.1 illustrates some of the potential applications of OE. A significant industrial interest is also growing in OE with established companies like Samsung, LG, Philips and Sony demonstrating several prototypes out of organic semiconductors [7]. Leading to the OE revolution, a number of OE-based startups, such as Plastic Logic®, Cambridge Display Technology®, Novaled® have also come into existence [8]. It is envisioned that, in the future, organic circuits can be printed as we print papers today.

The research in OE in the past decade has been focused on the improvement in the performance of organic devices. The first generation of organic semiconductors (OSC) suffered from low charge-carrier mobility and poor device characteristics. A lot of efforts have been focused on the growth, deposition, spin coating and optimization of other processes in order to fabricate a high performance device. Although these issues are far from being resolved, the concentrated efforts resulted in manifold improvements in the mobility of charge carriers in OSC that have now surpassed their contemporary mobility values in polycrystalline inorganic semiconductors. As the performance of OSCs improves the investigation of other pertinent issues, such as charge transport, contact resistance, stability, flexibility and novel device structures has become the focus of research.

1.3. Scope of Work

Ever since the discovery of conductivity in organic materials, the electrical characterization of organic semiconductors has been an active area of research. Error free measurements and correct interpretation of results have always been challenging tasks. The field of organic semiconductors has largely been dominated by chemists and material scientists, primarily due to the restricted availability of purified and high quality OSC. Years

of research have led to the standardization and commercialization of OSC to the extent that high quality and purified OSC are now available to the researchers from all fields.

Understanding the electrical characteristics of organic devices is a challenging task. Electrical characteristics of organic devices physically resemble the characteristics of inorganic devices; however, the underlying physics could be significantly different, due to their different basic nature. The focus of the work is largely on understanding the characteristics of the electrical transport measured in organic devices. We have chosen well-established organic semiconductors such as C_{60} and Pentacene, and performed experiments that seem crucial in understanding the physics of organic devices.

Electrical characteristics are studied using current voltage and capacitance voltage measurements. The conductivity and stability of organic devices determine the reliability of the electrical results. Conductivity has two components: mobility and carrier density. The mechanisms governing these two components have been studied in this thesis. Using organic semiconductor based metal-insulator-semiconductor diodes, we have analyzed the sources of charge carriers in OSC. In particular, we have studied the concept of unintentional doping and the impact of atmospheric exposure on OSC, through capacitance voltage measurements.

Mobility in OSC has been investigated under the perturbation of strain and temperature on organic field effect transistors. Flexibility, being the prime advantage of OE, charge transport under the influence of curling and twisting is an important case study. The OFETs are electrically characterized under the influence of strain due to curling and twisting. The results are used to develop the physical understanding of the charge transport in organic semiconductors.

For practical applications of organic devices, their performance and stability has to be studied under realistic ambient conditions. An organic device working in a practical environment should be able to withstand varied ambient temperatures along with the effect of self-heating. Most of the temperature studies on OSC have focused on a low temperature range. We have explored the electrical behavior in the above-room-temperature range. The operations of OFETs were studied at elevated temperature focusing on charge transport and device stability. Considering the flow of thought and the different experimental investigations conducted during the course of this Ph.D, the title of this thesis has been selected as "Understanding and Optimization of Electrical Characteristics of Organic Devices".

1.4. Thesis Layout

This doctoral thesis is based on the papers published as first author by the student, during the course of his PhD. It provides an overview of the efforts undertaken in order to gain a better understanding of the electrical characteristics of organic field effect transistors (OFET). The work has been structured in the following way:

Chapter 2 starts with a brief introduction to the organic semiconductors itself. It continues to elaborate on prominent charge transport mechanisms involved in carrier conduction. A brief review of the different electrical measurements frequently used in organic devices has been discussed and their theoretical background for understanding the results has been established. Further, one of the most popular organic devices, an OFET, is discussed in detail with emphasis on the device structure, fabrication and characterization methods.

Chapter 3 investigates the validity of the concept of unintentional doping often reported in organic devices. The pentacene based MIS (Metal-Insulator-Semiconductor) diodes are characterized through capacitance voltage (CV) measurements in ambient conditions to study the validity of Mott-Schottky analysis. Numerical simulations have been done to analyze the experimental results. An injection barrier based compact model has been given to explain the CV characteristics.

Chapter 4 illustrates the strain study on top gate organic field effect transistors (TG-OFET) using n-type organic semiconductor. It starts with the optimization of C_{60} films for the top gate configuration for highest mobility. The organic films were deposited at different substrate temperatures in order to change the morphology and improve the crystallinity. The optimized films were then used to fabricate TG-OFETs on a flexible substrate. The flexible OFETs were curled into different bending radius to apply strain and, simultaneously, the electrical characteristics are measured. The measured change in conductivity is used to understand charge transport in organic semiconductors.

Chapter 5 tests the electrical characteristics of pentacene-based OFETs at elevated temperatures in ambient conditions. The different charge transport studies have focused on low temperature measurements. The stability of pentacene films have been studied first in hot air environment through different material characterization techniques. The results have been analyzed to verify the stability of OSC. Next, the OFETs are electrically characterized while being heated up to 190 °C. Various observations about the electrical characteristics have been reported and a unified understanding has been presented to explain the results.

Chapter 6 summarizes the achievements during the research and discusses an outlook of future aspects.

At the end, in the series of Appendix A to E, experienced-based tips which accumulated during the experimental lab hours of this work have been presented.

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Chapter 2.

Fundamentals of Organic Semiconductors

The objective of this chapter is to provide a theoretical framework for the work done in this thesis. It presents a discussion on the fundamental properties of organic semiconductors important to understand charge transport. The discussion is extended to the two relevant devices for this thesis, organic MIS diodes and organic field effect transistors. The operating principle, important parameters and factors that affect their performance are presented.

2.1. Organic Semiconductors

Organic semiconductors (OSC), a new class of materials, have attracted lot of attention for their characteristics, such as flexibility, low processing cost, chemically tunable properties, and room temperature processing. These advantages of OSC are due to the large carbon content of these materials. Organic molecules mainly comprise carbon atoms, with other different elements such as hydrogen, oxygen, nitrogen, sulphur attached to carbon atoms. It leads to almost infinite possibilities to permute these atoms to synthesize different organic molecules with different chemical and physical properties. The electrical properties of these molecules can be tuned to be insulating, semiconducting [1], metallic [2] or even superconducting [3].

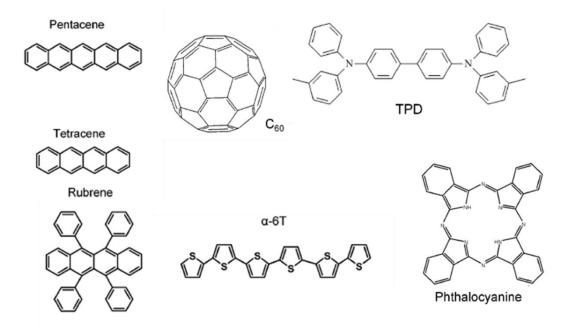


Figure 2.1 Chemical structure of small molecule organic semiconductors

Organic semiconductors can be broadly classified into two categories small molecules (or oligomers) and polymers [4]. Small molecules, such as pentacene, ruberene, tetracene and others, are commonly vacuum deposited to fabricate organic devices. Figure 2.1 shows the chemical structures of some of the most commonly used small molecule based OSC. Evaporation parameters of these OSC, such as the substrate temperature and, the deposition temperature; can easily be controlled, as a result this, small molecules generally result in high quality polycrystalline semiconductor films. The mobility in these films is frequently reported to be $1 \text{ cm}^2/\text{Vs}$ or above. Under optimized conditions, these molecules can align themselves to form organic crystals which are very useful in studying the intrinsic transport characteristics of organic semiconductors.

Polymers are long chain, high-molecular-weight organic semiconductors that are generally processed in wet conditions using techniques, such as spinning, spray coating and, ink-jet printing. Figure 2.2 shows the chemical structure of some of the most commonly used polymer-based OSCs. Polymer-based transistors generally have low mobility. These long chain molecules often twist among themselves, creating a random and inefficient network for charge transport. However, lately, there has been development in wet processing techniques such as Off-center coating, because of which, generates highly crystalline boundary domains. As a result the mobility in these materials are also reaching 1cm²/Vs and above [5].

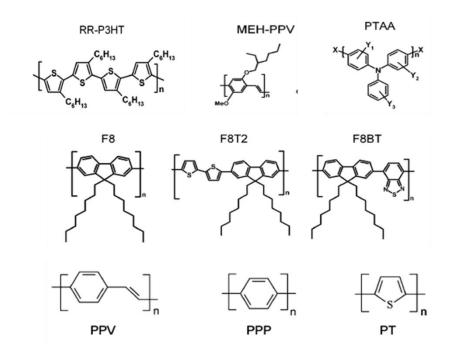


Figure 2.2 The chemical structure of polymeric organic semiconductors

Unlike inorganic semiconductors where polarity of the carriers in the semiconductor is decided through external doping, OSC are generally intrinsic and are used without any external doping. However, the applied gate voltage—negative for accumulating holes and positive for accumulating electrons—determines the polarity for OSC as p-type or n-type. The science behind the polarity of the OSC is not understood well. Although, experiments have shown that the chemical structure is not the only factor that determines the polarity of OSC. The other processing factors such as gate dielectric [6], and the choice of electrodes are also

crucial in determining the polarity of a working organic device [7, 8]. For instance, pentacene, in contact with a high work function metal (Au, Pd) results in p-type devices [9] and when in contact with a low work function metal (Ca), results in n-type conduction [10]. In cases where both types of metals are used as contact electrodes, ambipolar (both electron and hole type) kind of transport is observed [7].

2.1.1. Carrier Formation in OSC

Charge carrying ability of OSC is determined by the extent of conjugation present in these materials. In the different organic molecules shown in Figure 2.1, carbon atoms bind together covalently, with alternative single and double bonds. The unique abilities of carbon atoms—low electronegativity, small atomic diameter, and its ability to hybridize in sp, sp², and sp³ forms—determine the extent of conjugation in an organic molecule. The properties of the conjugated materials can be studied by analyzing the electronic structure of carbon atoms.

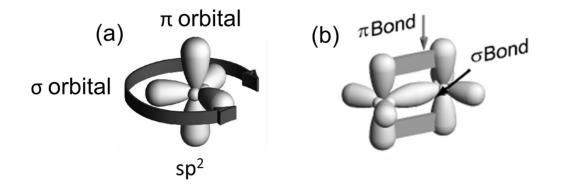


Figure 2.3 (a) sp² hybridized orbitals of carbon each σ orbital is at 120° from each other and π orbital is perpendicular to the plane (b) Orbital schematic of ethylene molecule showing σ and π bonds.

Six electrons are present in a neutral carbon atom. In the ground state, two electrons reside in 1s orbital, the other two in 2s orbital, and the remaining two occupy the 2p orbitals. The 2s and 2p orbitals are degenerate and are responsible for the way in which carbon atoms bind chemically to other atoms. In particular, when carbon atoms bind covalently to other atoms, mixing of orbitals happens, leading to hybridization. In a sp² hybridized carbon atom,

two single bonds and one double bond (like Benzene) are formed. In sp² hybridized carbon atoms, three sigma (σ) bonds are formed and are in the same plane with an angle of 120°, shown in Figure 2.3. They are strongly localized between two neighboring atoms and cannot move freely. The fourth p_z orbital overlaps in a plane perpendicular to the σ bond and form the pi (π) bond. Figure 2.3b illustrates the sp² hybridization in the C₂H₄ molecule. The π electron cloud is delocalized over the entire molecule and actively participates in charge conduction [11].

Molecular orbital theory predicts the formation of orbitals with distinct energy levels. In crystalline semiconductors, atoms are held together by strong covalent bonds, leading to hybridization of individual atomic energy levels resulting in energy bands. Organic molecules are held together by weak Van der Waal forces to from organic crystals. Compared to ionic and covalent bonds in inorganic semiconductors, Van der Waals forces are much weaker. This weak intermolecular interactions results in smaller wave function overlaps, and as a consequence, organic crystal has a narrow bandwidth of 0.5 eV compared to silicon, where valence and conduction bandwidth is of the order of 10 eV [11, 12]. In organics, the highest occupied molecular orbital (HOMO) is equivalent to the valence band and the lowest unoccupied molecular orbital (LUMO) has equivalence to conduction bands. However, though this model does provides an intuitive understanding, one should be cautioned that molecular orbitals do not represent the continuum of energy levels such as in inorganic semiconductors and the real picture is far more complex. The π -electrons are in HOMO level and can easily be excited to LUMO levels. It is due to these energies of π -electrons that the electronic properties of organic molecules are studied in terms of π -electrons [11]. Small bandwidths, strongly influence the charge transport in organic crystals making them sensitive to surrounding interactions from dielectric interface, molecular vibrations, disorder and other charge carriers. These factors strongly impact the charge carrier mobility and lead to new phenomena.

2.2. Organic Devices

Organic semiconductors provide an inexpensive alternative to fabricate electronic devices. The chemically tunable properties of OSC can provide tailor-made solutions for the requirements of different devices. In the early 90s, OSC had demonstrated different capabilities, such as generation of light and conversion of solar energy to electric energy

which were usually present in inorganic semiconductors. It led to successful demonstration semiconductors devices like organic field effect transistors, organic light emitting diodes, organic solar cells and such others. Over the years, these devices have been optimized for better performance and are now much closer to industrial production.

Of the many devices fabricated from organic semiconductors, the discussion has been restricted to the organic metal insulator semiconductor (MIS) diodes and organic field effect transistors (OFET). As will be shown, the two devices are interrelated. An overview of the structure and the working principle of the two devices are elaborated and the methodology to extract useful parameters is presented.

2.2.1. Organic Metal Insulator Semiconductor Diodes

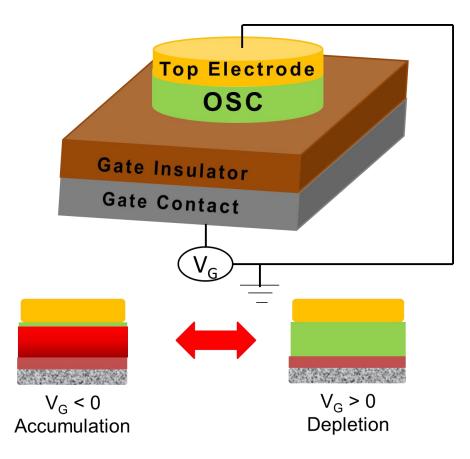


Figure 2.4 Schematic of an organic diode is presented. The charge statistics in the two states of the device is shown in two states of operation: accumulation and depletion. The graded red marking inside the green region is depicting the charge accumulation layer (deeper red at the interface signify dense accumulation) and empty green region signify depletion.

Metal Insulator Semiconductor (MIS) is a two-terminal device used for characterizing the interface, semiconductor and contact characteristics[13]. MIS diodes were very useful in understanding the Si/SiO₂ interface back in the 60s and 70s. MIS diodes and MIS capacitors are equivalent terms and have been used interchangeably in this thesis. In organic MIS diodes, an OSC is sandwiched between a dielectric layer and a top metal contact, with a back contact or gate contact deposited on dielectric. A better acronym for the structure would be MISM – metal-insulator-semiconductor-metal diode, however in order to draw correspondence with traditional silicon theory acronym MIS is used. Figure 2.4 shows a schematic of an Organic MIS diode and the charge states in different biasing at the gate electrode. An MIS diode allows us to individually probe the different region of operations–accumulation, depletion and inversion in typical semiconductor devices.

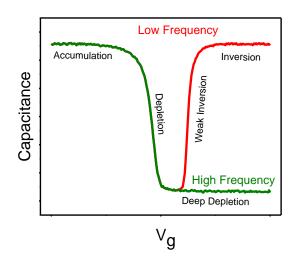


Figure 2.5 Typical capacitance voltage characteristics of silicon based MIS diodes observed at high frequency and low frequency. The different regions of operations are labeled in the figure.

MIS diodes are characterized using capacitance voltage (CV) measurements [13]. CV measurements can be of two types 1) Dynamic CV measurement, where AC bias is applied in addition to DC and the capacitance is extracted from the imaginary part of the impedance, 2) Quasi static CV (QSCV) [14], small DC voltage ramps are applied to the device and the accumulated charge is measured by integrating the current flowing in the device. The two methods are frequently used to calculate the capacitance in organic devices. QSCV measurement is more prone to noise compared to dynamic CV, whereas, the latter is strongly dependent on the frequency of the applied AC signal. OSC has low (0.1-1 cm²/Vs) mobility as

result the response time of the carriers is low, and so, CV measurements should be done at low frequencies (few kHz) to get the full response of the carriers. Appendix A lays out the useful details of the dynamic CV measurements used in this thesis.

For typical silicon-based inorganic MIS diodes, CV characteristics at different frequencies are shown in Figure 2.5. The CV transcends into different regions of operation as the gate voltage is swept from positive to negative. All three regions of operation are evident in the figure[13]. The frequency-dependent CV characteristics in the inversion region indicate the different response times of the inversion charges. Response time calculations were used to identify the source of inversion charges as the thermal generation in silicon based devices [13]. The CV characteristics of OSC-based MIS diodes can be different due to differences in the physical characteristics of two types of materials. Figure 2.6 shows the CV characteristics measured at different frequencies in organic MIS diodes. For a p-type organic device, a negative bias at the gate electrode leads to accumulation of holes at the interface (shown in Figure 2.4) and the capacitance will saturate to the maximum value of the dielectric capacitance, given by Eq. (2.1), where ε is the permittivity of air, ε_{ins} is the dielectric constant of the insulator and *A* is the area of contact and *d_{ins}* is the thickness of the dielectric.

$$C_{\max} = C_{ins} = \frac{\varepsilon \varepsilon_{ins} A}{d_{ins}}$$
(2.1)

$$C_{\min} = \frac{C_{ins} \times C_{OSC}}{C_{ins} + C_{OSC}}$$
(2.2)

As the gate voltage is increased to a positive voltage, charges will gradually deplete to form the depletion region and capacitance will corroborate to series a value of dielectric and OSC capacitance, Eq. (2.2). In organic devices, the inversion region is usually not achieved due to non-availability/generation of inversion charge or a slow response time [15]. While recording the CV measurements it is very important to pattern the semiconductor and the metal contact of the same size, as shown in Figure 2.6a. Otherwise, due to spillage of charge the area of the device will be uncertain. The capacitance in accumulation will not saturate even at a low frequency and will approach insulator capacitance asymptotically [16].

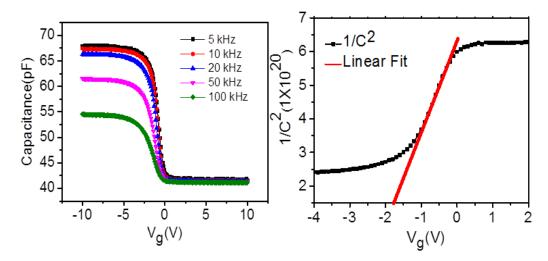


Figure 2.6 (a) CV characteristics of a pentacene-based organic MIS diode measured at different AC frequencies (b) Linear fitting of $1/C^2$ curve to extract the doping density (N_A)

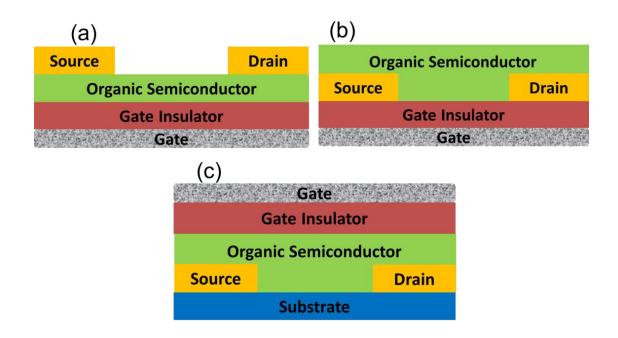
CV results are analyzed using Mott- Schottky (MS) analysis which exploits the linearity in $1/C^2$ -V curves to extract parameters such as the doping density (N_A), the built-in voltage (V_{bi}), and the depletion width (W) for OSC, using Eq. (2.3) and Eq. (2.4). Figure 2.6b demonstrates the usage of MS analysis. In doped silicon devices, the depletion of the dopant charges leads to formation of depletion region and hence the extracted N_A corresponds to doping concentration. OSC are often used without doping or at least without any deliberate doping. The extracted doping density is called unintentional doping density. The concept of doping density has been used since the early 90s to explain organic CV curves. It is often seen as the source of charges in OSC and used to explain different observations. However, the validity of MS analysis and unintentional doping has lately been challenged in several papers. In Chapter 3 of this thesis, the CV characteristics of organic devices are studied in detail and the understanding about unintentional doping has been extended.

$$\frac{\partial 1/C^2}{\partial V} = \frac{2}{\varepsilon_s q N_A A^2}$$
(2.3)

$$W = \sqrt{\frac{2\varepsilon_s (V_{bi} - V_A)}{qN_A}}$$
(2.4)

2.2.2. Organic Field Effect Transistors

The Organic Field Effect transistor is one of the most researched organic devices. It has two advantages mainly: first, it is an organic based switch device that can be used to build the circuits that derive the organic flexible display; second, it is an easy-to-fabricate test structure to study the properties of different types of organic semiconductors. In the section below, we discuss the principle of its working and the different factors to be taken care of.



2.2.2.1. Structure

Figure 2.7 (a) Bottom Gate Top Contact (BGTC) structure (b) Bottom Gate Bottom Contact (BGBC) structure (c) Top Gate Bottom Contact (BGBC) structure

OFETs have been demonstrated in many different and novel device architectures. The most commonly reported device architectures are shown in Figure 2.7. These are bottom gate/bottom contact (BGBC), bottom gate/top contact (BGTC) and top gate/bottom contact (TGBC). The structure of these devices differs, particularly, in terms of the fabrication sequence of the devices. For instance, in BGBC and BGTC, the metal electrodes are deposited before and after the OSC, respectively. The BGBC structures are advantageous, as lithography can be used in these structures to bring down the gate length, *L*. The top contact devices are usually deposited through shadow mask and the gate lengths are in few tens of microns due to physical limitations of the shadow mask.

The performance of the different designs discussed can vary significantly from each other. Any specific difference in the performance may be due to the difference in the semiconductor/dielectric interface and the ability of the contact to inject the carriers [17]. The interface in bottom gate devices is dependent on the surface roughness of the dielectric, whereas, in top gate devices it is dependent—as also shown later in the thesis—on the morphology of the OSC[18]. The contact resistance or the injection ability of the contact depends on the position of the electrode with the gate electrode. For instance, the BC devices offer more contact resistance compared to top contact devices. In TC devices, a large overlap area improves the injection, reducing contact resistance [19, 20].

Beyond these conventional structures, novel OFET architectures have also been explored. In a dual gate OFET, modification is made in BGTC structure to deposit a dielectric and gate from the top[21]. The channel in these devices can be controlled through two different gates that improve the electrostatics and hence the transport. Vertical transistors and other 3D designs have also been explored, however, due to the fabrication complexity, these architectures have never been prevailed.

2.2.2.2. Working Principle

OFET is a three terminal electronic switch in which the voltage on the gate electrode controls the conductivity of the channel in the semiconductor between the source and drain electrodes. It is an extension of MIS diodes with the top contact split in two (source and drain) electrodes separated by the distance of the channel length, L and the width W. The schematic of an OFET has been shown in Figure. Voltage is applied at the gate voltage (V_{GS}) and the drain voltage (V_{DS}) and the source terminal is usually grounded. Applied voltages are calculated with respect to the source voltage. Since the source is most negative compared to other terminal, it act as the source of electron that under the influence of the gate field accumulates at the gate semiconductor interface. The electric field between the drain and the source drives these carriers from the source to the drain, carrying the current (I_{DS}). Depending on the biases on the three terminals, the transistor operates in different regimes. Figure 2.8 illustrates the basic operating regimes.

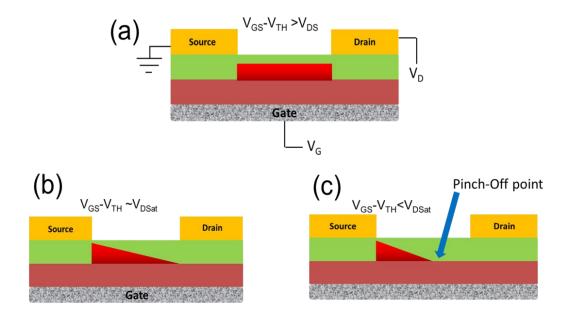


Figure 2.8 A Transistor working in the (a) linear region (b) near the saturation region (c) in deep saturation with the pinch-off point moving away from the drain terminal.

For a p-channel device, on applying the negative gate voltage, holes are accumulated at the dielectric/semiconductor interface. The density of the accumulated carrier is proportional to V_{GS} and the gate insulator capacitance, C_{ins} . However, all induced charges are not mobile. Organic semiconductor films are full of traps due to grain boundary disorder and interface defects. As the gate voltage is increased these traps are filled and the voltage at which this is achieved is called the threshold voltage, V_{TH} . The overdrive voltage (V_{GS} - V_{TH}) is the effective voltage that determines the free mobile current carrying carriers. When the applied V_{DS} is small ($V_{DS} << V_{GS}$), a uniform channel is formed and the I_{DS} is a linearly proportional to V_{DS} and the device is said to be operating in linear regime, as in Figure. The current voltage characteristics in the linear region are approximated using Eq. (2.5)

$$I_{DS} = \frac{W}{L} \mu_{lin} C_{ins} (V_{GS} - V_{TH}) V_{DS}$$
(2.5)

As the drain voltage is increased, it reaches $V_{DSat} = V_{GS}-V_{TH}$. It is the "pinch-off" point, at which, a small region near the drain goes below the threshold, due to local fields from the drain and the gate. The channel region is depleted of free carriers here and the space-charge-limited saturation current (I_{DSat}) flows. This region of operation is called the saturation region and the current voltage characteristics are given by Eq. (2.6). Further, increasing the V_{DS} increases the pinch-off region—effectively reducing the channel length. However, the

voltage at the pinch-off point is essentially the same as V_{GS} - V_{TH} and the current is saturated at I_{DSat} .

$$I_{DS} = \frac{W}{L} \mu_{sat} C_{ins} (V_{GS} - V_{TH})^2$$
(2.6)

2.2.2.3. Figures of Merit

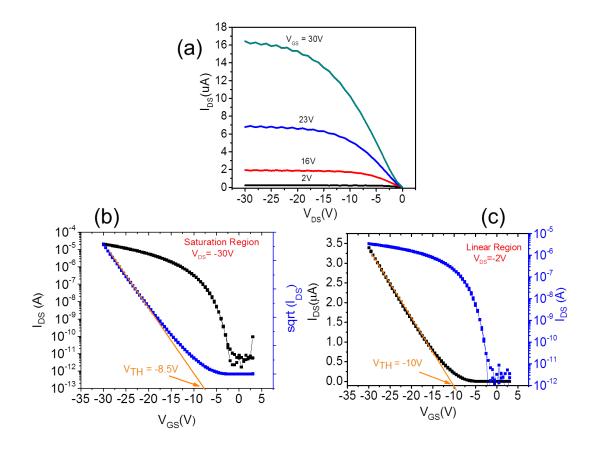


Figure 2.9 (a) Output (I_{DS} - V_{DS}) characteristics. Transfer characteristics (I_{DS} - V_{GS}) (b) in saturation region and (c) Linear region of pentacene based OFET fabricated during this thesis. $W/L = 700 \ \mu m/70 \ \mu m$

Figure 2.9 shows the typical output and transfer characteristics of a measured OFET fabricated during this thesis work. The different device parameters are given in the caption. The output characteristics in Figure 2.9a clearly show the linear regime at a low V_{DS} and saturation regime at a high V_{DS} . The transfer characteristics of the transistor biased in the linear region ($V_{DS} << V_{GS}$) and the saturation region ($V_{DS} \geq V_{GS} - V_{TH}$) are plotted in Figures 2.9b and c, respectively. From the semi-log plot one can see the exponential rise in I_{DS} below the subthreshold region in the two regions. For circuit designs, an OFET is characterized by four

device parameters—Mobility(μ), Threshold Voltage (V_{TH}), Subthreshold Slope (SS) and I_{ON}/I_{OFF} . The four parameters can be extracted from Eq. (2.5) and Eq. (2.6) depending on the biasing condition.

Mobility is one of the most important parameters that characterize the organic semiconductor and can be extracted through different methods. The mobility measured from the different techniques tends to vary depending on the device architectures. OSC are low mobility and low carrier density materials. Applying the gate voltage increases the charge density, filling the deep traps; as a result, the measured mobility in OFETs is higher than the mobility measured through techniques.

The mobility measured through the transistor could either be effective mobility (μ_{eff}) measured from the drain conductance using Eq. (2.7) from Figure 2.9a or field effect mobility (μ_{FE}) measured from transconductance using Eq. (2.8) [22]. Although both types of mobilities are measured in the same device, but due to the gate voltage dependence of the mobility, their magnitude tends to vary.

$$g_{DS} = \frac{\partial I_{DS}}{\partial V_{DS}} \bigg|_{V_{GS}} \sim \frac{W}{L} \,\mu_{eff} C_{ins} (V_{GS} - V_{TH})$$
(2.7)

$$g_{m} = \frac{\partial I_{DS}}{\partial V_{GS}} \bigg|_{V_{DS}} \sim \frac{W}{L} \mu_{FE} C_{ins} V_{DS}$$
(2.8)

In different mobility studies reported for OFETs, it is common to use field effect mobility. μ_{FE} can be calculated in the linear region using Eq. (2.8) or in the saturation region using Eq. (2.9). Eq.(2.9) is under the assumption that the mobility is independent of gate voltage.

$$\mu_{FE,sat} = \frac{2L}{WC_{ins}} \left(\frac{\partial \sqrt{I_{DS}}}{\partial V_{GS}}\right)^2$$
(2.9)

The threshold voltage is another important device parameter. Its microscopic understanding is not very clear, however, it is empirically defined as the voltage at which the channel conducts sufficiently. It is useful in digital design in defining the On and the Off state

of the device. The threshold voltage of the device depends on the semiconductor, the dielectric[23], trapped charges[24], the built-in dipoles[25], interface states, the injection barrier, the thickness of the semiconductor[26] among other factors. It can be extracted from Figure 2.9c by linearly extrapolating the square root I_{DS} with the V_{GS} .

The subthreshold slope of the device determines the switching speed of the transistor. The change needed in the gate voltage for per decade increase in the drain current is defined as the subthreshold slope. It is calculated using

$$SS = \left[\frac{d\log(I_{DS})}{dV_{GS}}\right]^{-1}$$
(2.10)

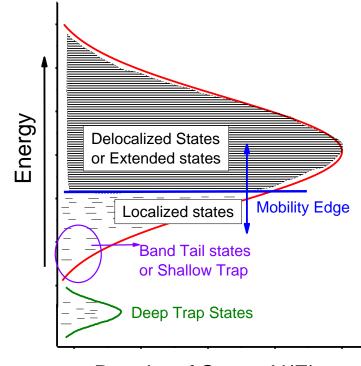
SS depends on the gate capacitance and trap states at the interface [27]. OFETs usually have a very high value of SS in the range of a few volts [28], however, very optimistic values have also been reported [29]. According to the IEEE standards [30], the I_{ON}/I_{OFF} ratio is defined as ratio of the maximum value of I_{DS} to the minimum value I_{DS} . It does not need to be at "0" gate voltage as the threshold voltage can shift the off state of the device to a higher or a lower value.

2.3. Charge Transport Models

The motion of the charge carriers inside organic semiconductors are described using two sets of contrasting ideas. Charge transport in highly ordered organic crystals is assumed to be band like transport—usually reported in highly crystalline silicon semiconductors [31]. On the other hand, charge transport in disordered semiconductors is described by thermally activated hopping of carriers through the distributed localized states or shallow traps [32]. It is difficult to formulate a unified theory of transport for OSC that can address the effect of different type of disorder present in organic semiconductors. The different types of disorder present in thin films can severely impact the density of states in OSC. In the following sections, an understanding of the density of states in OSC is presented along with a discussion on most commonly used charge transport models. The detailed reviews on charge transport can be found in Ref. [4, 33-35].

2.3.1. Density of States Model

Covalently bonded crystalline semiconductors have well defined delocalized energy bands separated by a forbidden energy gap. The charge carriers are delocalized within these extended states and move freely, only limited by scattering. In contrast, organic semiconductors are weakly bonded, held together by weak Van der Waals forces. The loss of long range order results in absence of translational symmetry in three dimensional periodic lattices of disordered films. It results in a random distribution of potential wells yielding a distributed Density of States (DOS) [36, 37]. In polycrystalline films, a partial range of order exists whereas amorphous films are completely dominated by strong localization and energetically distributed states. The charge carrier transport in organic systems occurs through incoherent hopping within the DOS. The structural disorder tends to introduce shallow localized states, also called band tail states. The deep localized states are due to topological and chemical impurities. The charge transport in polycrystalline films is usually described within the interplay between the localized and the delocalized states [36-38].



Density of States N(E)

Figure 2.10 Schematic of the typical density of states in disordered semiconductors. Mobility edge separates between the localized states and the extended states.

Figure 2.10 shows the typical density of states distribution in OSC. It is hypothesized that for the charge in the middle of the band far above the band tail, the effect of disorder will be weak. The states in the middle of the band are extended and the band tail states are localized. Mott introduced an important parameter called mobility edge which separates extended states and the localized states [39, 40]. If the Fermi level is below the mobility edge, the conductivity will be negligible. As the Fermi level passes the mobility edge, conductivity is expected to improve [39, 41]. As the disorder is increased, the extended states will start to localize and the mobility edge will move up in the band. In highly disordered films, the disorder width can exceed the bandwidth of extended states and the entire band is localized. The charge transport in amorphous organic semiconductor films is characterized by the disorder width and mobility edge. The density of states in disordered semiconductors can be modeled using different mathematical expressions. The three models that are frequently used in literature to study charge transport are constant DOS[41], exponential DOS[42] and Gaussian DOS[36] depending on the increasing computational complexity.

2.3.2. Multiple Trapping and Release Model

The multiple trapping and release (MTR) model assumes that a narrow band of high density localized states associated with traps exist near the delocalized levels. These are temperature dependent trap sites and can dominantly control the charge transport mechanism in disordered semiconductors [43]. Transport of charge carrier happens through successive trapping and release events. Different reports have used the MTR model to explain the thermally activated Arrhenius behavior observed in the OFET mobility, using the form

$$\mu \propto \exp(\frac{\varepsilon_T}{k_B T}) \tag{2.11}$$

where ε_T is the energy of the trap level below the mobility edge, or a characteristic trap energy for an energetic distribution of traps. The MTR model can also explain the gate bias dependent mobility often observed in OFETs [44, 45]. In many cases, the MTR model did explain the behavior of the mobility in OFETs; however, it is difficult to accept its generality for organic polymers. The MTR model requires uniform distribution of traps in space combined with delocalized electronic states, both of which are unlikely to occur for disordered OSCs.

2.3.3. Hopping Model

Hopping is defined as the thermally activated tunneling of carriers between localized states, rather than by the activation of carriers to a transport level. In disordered organic semiconductors, bands are visualized as a collection of localized states that are distributed spatially and energetically. Charge conduction happens through the hopping of carriers between these localized states. In a variable range hopping (VRH) model charges can hop a short distance with high activation energy or long distance with low activation energy [42, 46]. Hopping is a statistical phenomenon captured by Miller and Abrahams' jump rate equation [47]. It is a phonon assisted phenomenon which occurs by absorption and desorption of phonons to overcome the energy barrier between localized states.

Different mobility models have been developed to rationalize the hopping transport. The temperature dependence of mobility is of the form

$$\mu \propto \exp[-(\frac{T_1}{T})^{1/\alpha}]$$
(2.12)

where α is an integer ranging from 1 to 4 depending on the DOS model and dimension of the system used [42]. For a 3D uniform constant DOS, α is equal to 4.

The VRH model can successfully predict the gate voltage dependence and the temperature activation of mobility often observed in OFETs. As the gate voltage is increased, the accumulated charge carriers fill the lower lying states in the OSC and any additional charges in the accumulation layer occupy states at relatively high energies. Consequently these additional charges will require less activation energy to hop between the sites [42].

2.3.4. Polaron Model

Charge transport in OSC can also be affected by the formation of polarons. Charge carriers moving in an ionic or polar semiconductor, can polarize the surroundings, forming a polarization cloud that will propagate along with the carriers. The carrier and its polarization cloud can then form a quasi-particle, which is called a polaron [48]. A schematic representation is shown in Figure 2.11 The distortion of the polarized medium "attracts" the electron and tends to slow down the electron significantly; this is because, if the electron moves, the distortion is forced to follow. The coupling between the electron and the surrounding cloud depends on the polarizability of the material and the width of the conduction/valance band. In organic semiconductors; this makes OSCs much more sensitive to polaronic effects[33, 48].

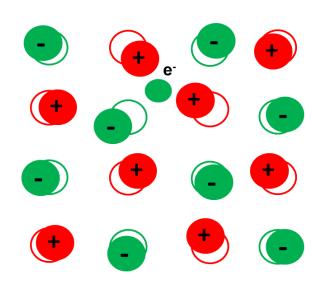


Figure 2.11 Schematic representation of the formation of a polaron. The presence of an extra electron in a crystal distorts its surroundings due to columbic attractions.

The charge transport in OSC can also be affected by the formation of polarons. The charge carriers moving in ionic or polar semiconductor, can polarize the surrounding forming a polarization cloud that will propagate along with the carriers. The carrier and its polarization cloud forms a quasi-particle, which is called polaron [48]. A schematic representation is shown in Figure 2.11 The distortion of the polarized medium "attracts" the electron and tends to slow down the electron significantly because if the electron moves, the distortion is forced to follow. The coupling between the electron and the surrounding cloud depends on the

polarizability of material and the width of conduction/valance band. In organic semiconductors polarizability is large and narrow bandwidths compared to inorganic semiconductors, which makes OSC much more sensitive to polaronic effects[33, 48].

In OFETs, the charge transport happens near the semiconductor insulator interface. The charges in the accumulation layer polarize not only the organic crystal but also the lattice in the gate insulator. Such kinds of polarons are called Fröhlich polarons. The coupling strength of Fröhlich polarons depends on the polarizability of the dielectric materials. Using different dielectrics with different polarizability can tune the strength of the coupling from weak to strong[49]. In case of strong polarization, the charge carriers form a dielectric polaron. When the radius of the polaron is comparable to the spacing of the lattice, transport close to room temperature occurs through incoherent hopping between neighboring molecules. For strongly coupled Fröhlich polarons of a small radius, the temperature dependent mobility is given by [49, 50]

$$\mu \propto \frac{a}{\hbar} \frac{\omega_s}{T} \exp(\frac{-\Delta}{T})$$
(2.13)

where *a* is the hopping length between neighboring molecules, \hbar is planck constant and ω_s is the phonon frequency [50]. The polaron-based model also predicts the thermally activated mobility in OFETs.

2.4. Role of Contact electrode

Organic Semiconductors are typically are high band gap (2-4 eV) semiconductor. The source of charges in these materials is primarily through injection from the contacts. Unless extrinsically doped, OSCs are low carrier density materials and due to high disorder and low mobility, the charge transport in these materials is mostly bulk limited. However, for OFETs, under accumulation, charge carrier density at the interface increases and transport is no longer bulk limited but can be restricted by the injection of charges from the contacts. The improvement in the performance of OFET has made the contact resistance an important issue for low mobility organic devices [51].

The physics of charge injection is not very well understood as several convoluted factors are expected to be responsible [52]. Empirically, injection at the metal organic interface depends on the device geometry, quality of the interface and the Fermi level alignment. The different OFETs structure shown in Figure 2.7 leads to different contact resistance [53, 54]. In top contact devices, when the metal contact is deposited on top of OSC it leads a conformal deposition and better interface, lesser trap density compared to the BC device [51]. In addition, a large overlap area between the contact and gate increases the charge injection compared to bottom contact devices where injection is primarily from the sides [55]. The three dimensional device architectures are expected to behave differently with respect to charge injection [56, 57].

The other methods of metal semiconductor contact improvement are contact doping [58], work function alignment (W.F.)[9], contact modification through self-assembled monolayers[59]. The injection ability of the electrode is determined by the Fermi level alignment at the metal semiconductor interface. A simplified Mott-Schottky rule predicts the injection barrier (ϕ) as the difference between the metal work function (W.F) and the HOMO or LUMO level of the semiconductor [60]. If the injection barrier at the interface is less, for example gold (W.F = 5.1 eV) and pentacene (HOMO = 5.0 eV), a good ohmic behavior is expected. However with Al $(W.F.=4.1 \ eV)$ a non-injecting contact is formed. There are exception to this rule like with Cu (W.F.=4.4 eV), pentacene does form a good ohmic contact[61]. It is predicted at metal semiconductor interface, dipoles are induced which alter the W.F. of the metal and the resultant injection barrier. The other contact improvement methods like contact doping [58] and SAM [62] layers effectively aims at altering the dipoles at the metal semiconductor interfaces. Several UPS based studies have verified the existence of such dipoles [60, 63]. Dipoles at the interface can be formed due to environmental contamination, change in morphology, interface defect and other extrinsic affects [60, 63]. Although, deliberately engineered dipoles at the interface through techniques like selfassembled monolayers [59, 62], interfacial oxides [64, 65], doping can effectively reduce injection barrier.

Contact resistance (R_C) can be characterized through different techniques [66, 67] although the most prevalent one is transfer line measurement (TLM) [54]. The different OFETs are fabricated with same width (W) and different channel length (L). The contact resistance can be extracted using Eq. (2.14) where R_{TOT} is total transistor resistance in linear regime and all other parameters have their conventional meaning.

$$R_{TOT} = R_{Ch} + R_C = \frac{L}{WC_{ins}(V_{GS} - V_{th})\mu_{ch}} + R_C$$
(2.14)

2.5. Role of Gate Dielectric

The gate dielectric plays an important role in controlling the different OFET parameters and has been thoroughly investigated in the literature [68, 69]. The charge transport happens at the dielectric semiconductor interface, and as a result, can be influenced strongly by the physical and chemical properties of the dielectric. The accumulation charge depends on capacitance due to the dielectric, given by $C = \varepsilon \varepsilon_{ins}/t_{ins}$. An optimal choice of dielectric will have low thickness (t_{ins}) and a high dielectric constant (ε_{ins}) with high field strength. Other physical characteristics of dielectric that are of practical importance are low surface roughness to have uniform morphology with large grains[18], no trapped charge to reduce hysteresis[70], thermal and air stability and, simultaneously retaining the desired flexibility in OFETs[28, 68].

Typically, the gate dielectric can be inorganic, organic, or a combination of both inorganic and organic. Inorganic dielectrics, generally oxides, typically have low leakage current and high dielectric constant but they tend to form a bad interface with OSCs having lot of defects[69, 71]. The high dielectric constant induces energetic disorder in weakly bound OSCs, leading to formation of polaron [49], thus, hindering the transport. Additionally, inorganic dielectrics are brittle and offer limited flexibility. Organic dielectrics like PS, PMMA, PVP and the like are better suited for OFETs in terms of interface compatibility and flexibility [72, 73]. They also offer low cost processing solution in form on spin coating[74] or printing[75]. However, the organic dielectrics have less dielectric constant and a weaker dielectric strength does not offer the most reliable OFETs. Consequently, hybrid dielectrics are frequently used in OFETs to optimize the best of both worlds [76, 77]. A thin inorganic dielectric layer is deposited through techniques such as anodization or sputtering providing high dielectric strength [78, 79]. On top of these, a thin layer of organic dielectric is used to provide a good interface to the OSC[73]. The top organic layer can also be replaced with few nanometer SAM layer which help in increasing the overall capacitance[80]. Such devices can operate at very low voltages [80] and have been successfully demonstrated for various applications [79, 81].

2.6. Stability

As the technology for the fabrication of OFETs is improving, gradually, the interest is shifting towards the study of the reliability and electrical stability of OFETs under realistic ambient conditions [82, 83]. A reliable OFET will require stability in threshold voltage, hysteresis-free characteristics and long term bias stress operational stability without degradation [84]. The stability of OFETs can be studied either in terms of semiconductor degradation or the degradation of the OFET characteristics. In some sense, the latter is the manifestation of the first, however, the fact that the OSC itself degrades implies that engineering efforts cannot improve the stability; while, if it is the latter, process engineering can significantly improve stability.

OSCs such as C_{60} , P3HT and, Pentacene are reported to suffer from chemical instabilities on exposure to atmosphere and light[85, 86]. In the presence of oxygen and moisture, there are H+ ions, OH- ions which can either oxidize or reduce the OSC. The ability of OSCs to either oxidize or reduce depends on their reaction potential[87]. It is desirable that hole conducting materials have a deep HOMO level (> 5.2 eV) [88] and electron conducting materials have high electron affinity (>3 eV) [89]. Pierels instability predicts that the extent of conjugation in these material also affect their stability by decreasing the band gap [11, 90]. The chemist and material scientist are on the constant look out for more stable and high mobility organic semiconductors [32]. The two such alternatives which are attracting lot of attention are DNTT [81] [91] and TIPS pentacene [5, 31].

Extrinsic factors such as presence of impurities and moisture, interface defects, structural and energetic disorder of the semiconductor are responsible for the electrical instability of OFETs. The presence of mobile ions in the dielectrics can shift threshold voltage and cause hysteresis. However, the presence of interface traps results in stretching of current voltage characteristics and degradation of the subthreshold slope. Humidity tends to exacerbate the degradation rate [92]. Operating the device for long durations can result in threshold voltage instability due to trapping [93]. Bias stressing the device for the longer duration can generate localized traps in the semiconductor, insulator or at the active interface [94, 95]. These trapped charges remain in the films even on switching off the device. In a few cases where the device was left for long hours, its operations were restored. Such restoration is accelerated due to annealing [96] or in presence of light due to quenching of excitons [97].

The instability observed in OFETs is difficult to segregate from between the two types discussed earlier. As a result organic devices face lot of perception problems. Usage of compatible processes can greatly improve the stability of OFETs. Non polar organic insulators such as PS are very useful in reducing the effect of hysteresis. A layer of non-polar dielectric not only passivates the oxide traps but also limit the moisture content. Recently, a new class of naturally occurring materials such as indigo dye has been reported to give environmentally stable OFETs [98, 99]. These materials have shown prolonged stability in air, with stable performance. The different reliability studies have explored the stability primarily under ambient conditions and under bias stress. The high temperature stability of OFETs also represents a case study of practical importance largely ignored so far. In this thesis, the stability, from the device and semiconductor perspective at elevated temperatures has been studied.

2.7. References

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Chapter 3.

Role of Injection Barrier in Capacitance Voltage measurements in Organic Devices

The operation of organic electronic devices is often understood by invoking the concept of "unintentional doping". However, the applicability and usefulness of this controversial concept is not very clear and is under much recent debate. In this chapter, we have revaluated the validity of this concept through careful experiments and detailed numerical simulations. Specifically, we have used use the Capacitance Voltage (CV) measurement of pentacene devices as a testbed to unravel the role of injecting electrodes and unintentional doping (if any).

3.1. Introduction

The field of organic electronics has witnessed remarkable technological advancement in recent years; however, the understanding of the underlying physics has been lagging in many aspects. One such controversial idea is related to depletion region formation in organic semiconductors (OSC) due to unintentional doping [1-6]. Although, both Capacitance Voltage (CV) and/or Two probe (or Four probe) resistivity measurements (or current-voltage, I-V, measurements) can be used to study the effect of doping in semiconductors, IV measurements are influenced by both carrier density and mobility; an increase in either of the parameters will result in an increase of current. On the other hand, CV measurements are more sensitive to carrier density alone and the associated Mott-Schottky(MS) analysis [7, 8] exploits the linearity in $1/C^2$ -V curves to extract parameters such as doping density (N_A), built-in voltage (V_{bi}), and depletion width (W) for OSC, using Eq. (3.1)-(3.2).

$$\frac{\partial 1/C^2}{\partial V} = \frac{2}{\varepsilon_s q N_A A^2}$$
(3.1)

$$W = \sqrt{\frac{2\varepsilon_s (V_{bi} - V_A)}{qN_A}}$$
(3.2)

Traditionally, CV has been a well-established technique to measure doping density in inorganic semiconductors [9], and in the early 90's it was adopted for organic semiconductors [8, 10]. However, the origin of dopants in organic materials is complex and the values of doping densities extracted from MS analysis and reported in literature vary drastically. For example, in one study, the dopant density has been reported to be insignificant [11], whereas, it has been used to account for the various observed results in other reports. [1, 12] In the absence of any intentional doping, [13-15] the linearity in $1/C^2$ -V behavior has been explained by assuming that organic semiconductors are "unintentionally" doped [1, 8, 11, 16]. However, the sources of such doping are not well established. While oxygen and light have often been reported as being critical factors [5, 16-18], surprisingly, unintentional doping has been attributed even for devices fabricated inside a glove box with an inert ambience [7, 11, 12, 19]. The values of unintentional doping density reported vary from 10^{14} - 10^{18} cm⁻³ depending on the thickness of the OSC used.[11, 16] While the lower values are apparently insignificant,

higher values are matter of concern as they influence the formation of a depletion region inside the OSC. Accordingly, a large variation in depletion thickness—from few nanometers [20, 21] to the full thickness of the OSC [11, 19] has also been reported. Amid these debates, Kim *et al.*[11] have shown that depletion capacitance in pentacene does not have voltage dependence even for thick films (1 μ m thickness). In another interesting work, Kirchartz *et al.*[22] have raised doubts about the sensitivity of Mott-Schottky analysis for thin film organic diodes. However, due to lack of an alternative explanation for the Mott-Schottky behavior (apparent linearity in 1/C²-V plot), the unintentional doping concept has been continuously used to explain and quantify the physics of organic devices. At the same time, the critical role of contacts on capacitance measurements has not been understood well. Although there have been some related reports, [23] quantitative studies on this aspect are still lacking, especially for thin film organic devices.

3.2. Experimental Details

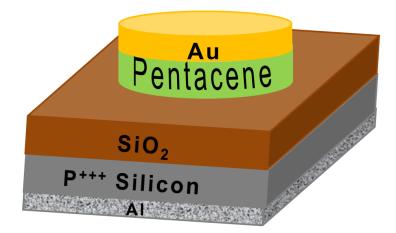


Figure 3.1 Device Schematic of MIS structure

A highly doped P-type silicon wafer of resistivity 0.0001 ohm-cm was used as a substrate. At such a low resistivity, the silicon substrate can also be treated as metal due to a very small depletion width (few nm). A high quality oxide of 66 nm was thermally grown on it. Back-side oxide was etched and aluminum was deposited as the substrate contact metal. Pentacene, triple sublimed with 99.9% purity from Sigma Aldrich, was evaporated using a shadow mask with a deposition rate of 0.2 nm/s. Pentacene of a thickness of 62 nm was confirmed using the Ambios profilometer. On the same substrate, in the separate regions,

aluminum and gold contacts were evaporated using the same shadow mask, to ensure uniformity in the thickness of the Pentacene. The resultant device was a well-patterned MIS structure, as shown in Figure 3.1. The device area is approximately $1.3x10^{-3}cm^2$. The Keithely 4200 semiconductor characterization system and the HP 4284A LCR meter were used for device characterization. The voltage was applied at the bottom electrode while the top contact was connected to the ground. The capacitance was extracted from the imaginary part of the measured complex admittance using a parallel combination of capacitance and the conductance model (C_p-G_p model) [24]. Note that the entire device fabrication and characterization was conducted in an ambient atmosphere with humidity of 55% and at room temperature. The results presented in this work represent a typical dataset measured over multiple samples in different runs.

3.3. Results

3.3.1. Contact Dependent

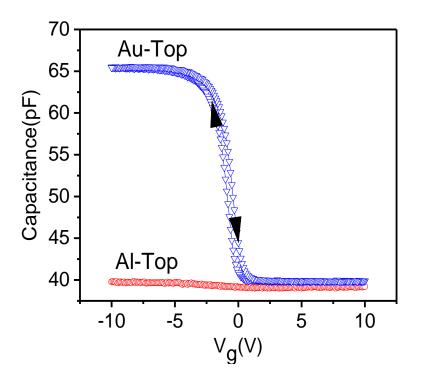


Figure 3.2 Capacitance Voltage characteristics for Pentacene capacitors with aluminum and gold contacts measured at 10 kHz

Figure 3.2 shows measured CV characteristics for two top metal contacts. The measurement frequency was 10 kHz and no hysteresis was observed. For gold contact devices, the capacitance shows an apparent transition from accumulation to depletion. The capacitance at negative biases saturates to a value close to oxide capacitance (C_{ox}) given by Eq.(3.3), while for positive biases, it reaches a constant value of C_{min} , equivalent to series capacitance of oxide and Pentacene ($C_{pentacene}$), given by Eq.(3.4). Surprisingly, the usually expected accumulation behavior is not observed in aluminum contact devices. Here, the capacitance is more or less constant for the entire range of the applied gate voltage and did not increase even for lower frequencies.

$$C_{\max} = C_{ox} = \frac{\mathcal{E}_{ox}A}{d_{ox}}$$
(3.3)

$$C_{\min} = \frac{C_{ox} \times C_{pentacene}}{C_{ox} + C_{pentacene}}$$
(3.4)

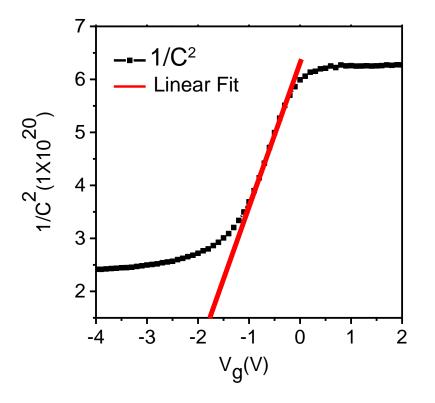


Figure 3.3 Mott-Schottky analysis of Au contact CV characteristics to extract N_A and V_{bi}

For the gold contact, capacitance perfectly correlates with the deposited oxide and pentacene thicknesses. The dielectric constant of pentacene was found to be 5 (back extracted from C_{min} , see Eq.(3.4)). Although lower values of the dielectric constant are typically used,[11] higher values of the dielectric constant of Pentacene was also reported in the past [25, 26]. Using the traditional Mott-Schottky analysis over the transition region, Figure 3.3, we obtained the doping density, $N_A = 8x10^{16} \text{ cm}^{-3}$ and built-in voltage, $V_{bi} = -1.6 \text{ V}$. Since we have not intentionally doped pentacene with acceptors, the observed doping density has been traditionally called "unintentional doping", corresponding to a p-type inorganic device. The built-in voltage corresponds to the internal electric field which corresponds to the uncovered charges of the dopants. It is believed that oxygen and moisture from the ambient environment during the processing might dope Pentacene, thus, generating free carriers and ionized dopants [8, 18]. However, it is difficult to comment on the validity of atmospheric doping since for $N_A = 8x10^{16} \text{ cm}^{-3}$ dopants, 62 nm of Pentacene will be fully depleted at $/V_{bi}$ - V/\sim -1.6V, which is seen in Figure 3.2.

3.3.2. Atmospheric Degradation

The gold devices were periodically measured to study the impact of ambient exposure on CV characteristics. Figure 3.4 shows the CV characteristics measured at 10 kHz frequency. A freshly prepared device shows complete transition from C_{ox} to C_{min} . It should be noted that the characteristic CV shape is due to depletion in pentacene and not due to depletion in silicon, which is highly doped. The maximum value of the capacitance (C_{max}) gradually degrades from C_{ox} to lower values over 50 days, while almost no change is observed in C_{min} . Similar results have also been reported by Akhtaruzzaman et al.[27], however, the observation lacked proper justification. As mentioned before, the most common explanation for organic CV curves has been based on doping by atmospheric oxygen and moisture [7, 11]. Figure 3.4b and c show the extracted dopant density extracted using Eq. (1) for a fresh device and the device characterized after 50 days of ambient exposure, respectively. The doping density seemingly increases from 6.6×10^{16} cm⁻³ for the fresh device to 3.1×10^{17} cm⁻³ with 50 days of atmospheric exposure. Although the calculation shows an increasing doping density, it is contrary to degrading C_{max} values. With increasing dopant density, one would expect an increase in C_{min} due to reduction in depletion width or an increase in voltage (more positive, in our case) at which the full depletion is attained-either of which is not the case in Figure 3.2. On the other hand, a change in C_{max} is not consistent with the increased atmospheric doping.

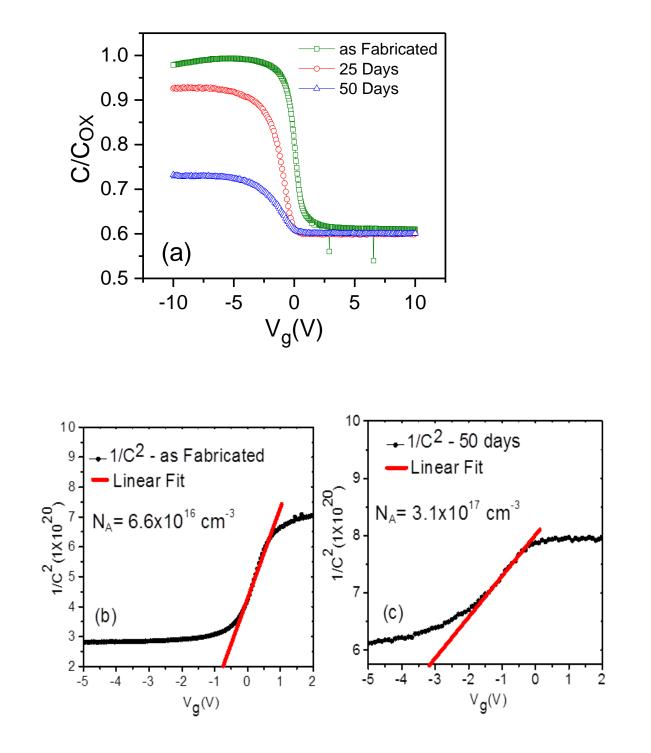


Figure 3.4 (a) CV characteristics measured in prolonged atmospheric exposure (b) and (c) show the extracted doping densities from the MS analysis for as-fabricated and devices ambient exposed for 50 days, respectively.

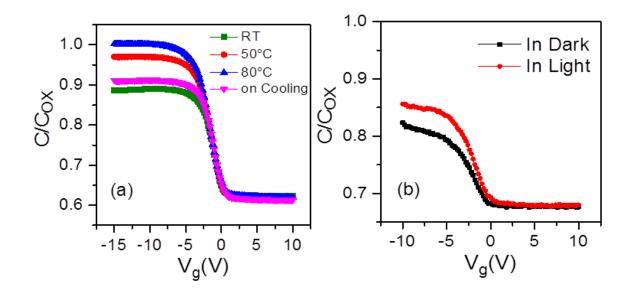


Figure 3.5 Measured capacitance voltage characteristics on (a) heating (b) under illumination

Further, the exposed devices were investigated for thermally activated dopants and under illumination for photo-induced doping [18], shown in Figure 3.5a and b, respectively. Upon heating, C_{max} gradually recovered to C_{ox} at 80°C and collapsed back to its initial value on cooling, indicating that the effect of the exposure is permanent. A similar change, although smaller in magnitude, is seen under illumination. In both, Figure 3.5a and b, C_{min} is fixed at a constant value and C_{max} changes. It should be noted that the effect of light is limited in these devices due to the restricted entry of light from the sides only. The effect of light was partially reversible. Nevertheless, the results aid in illustrating that the light affects the C_{max} more significantly than C_{min} , which is possibly interpreted as photo-induced doping[18]. The constant values of C_{min} indicate that the conventional inorganic definition of doping cannot be generalized for atmosphere exposed pentacene devices. The derived interpretation of the increasing doping density from the MS analysis (1/C²-V) fails to explain experimental results, and hence, needs to be carefully used [28].

3.4. Role of Contacts

3.4.1. Theoretical perspective

Insights into device operation and the relevance of the concept of "unintentional doping" can be obtained from the analysis of the accumulation regime. As is evident from Figure 3.2, the capacitance saturates to C_{ox} for large negative voltages. For an applied bias of -10V, the accumulated hole carrier density in the device $(Q=C_{ox} V)$ is of the order of $3x10^{12} \text{ cm}^{-2}$. If we assume that the device indeed had an unintentional doping density of $N_A=8x10^{16}\text{ cm}^{-3}$ (as suggested by the MS analysis, Fig. 1), the maximum hole density contributed by the 62 nm-thick pentacene towards the accumulation condition is limited to about $5x10^{11} \text{ cm}^{-2}$ (note that this analysis assumes ideal conditions—zero traps, complete ionization of dopants, negligible depletion region at the top metal/OSC interface and the like). This means that there is almost an order magnitude of deficit in charge in the device and it is evident that the required excess charge has to be supplied, either by thermal generation or through contact injection. We can neglect thermal generation since Pentacene is a relatively large band gap material (band gap 2.4eV). Thus, the only available source of accumulation charge in pentacene is through contact injection.

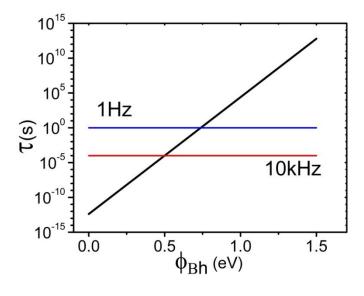


Figure 3.6 Response (Injection) time (τ) to inject $10^{-9} C/cm^2$ charge for different injection barrier (Φ_{Bh}). 10 kHz and 1 Hz horizontal cut indicate the barrier below which the injected charge will respond to the respective frequency.

In addition to the net charge in the device, the response of the perturbed charges with respect to applied ac frequency plays a critical role in CV measurements. The response time of the injected carrier depends on the injection time associated with the respective contact injection barrier. [29, 30] For an applied ac bias (80mV), perturbed charge carriers (Q_{pert}) is of the order of 10^{-9} Coulombs/cm⁻² (Q=CV) in the accumulation regime. The current injection from the contact should be able to support this charge such that eq. (3) is satisfied. According to the thermionic emission model, [9] the injection current from the metal to semiconductor is independent of bias and is given as $J = A^{**}T^2 \exp(\frac{-q\phi_{Bh}}{kT})$ where A^{**} is the Richardson constant calculated to be 0.12 A $cm^{-2} K^{-2}$ for pentacene, [29, 30] T is the temperature, k is the Boltzmann constant and ϕ_{Bh} is the injection barrier height for the hole. Here the term ϕ_{Bh} is used for hole transport and denotes the difference between the HOMO level (ionization potential) and the metal work function. From this, the expected response time for contact injected carriers can be defined as $\tau = Q_{pert}/J$. Figure 3.6 plots the response time (τ) corresponding to various values of Φ_{Bh} for injecting the required charge. For $\phi_{Bh} = 0$ to 0.5 eV, au is less than 10⁻⁵ s, and therefore, the injected charge will be able to respond to all frequencies less than 10 kHz. The work function of gold in literature varies from 4.9 eV to 5.2 eV [11]; therefore, the 10 kHz frequency is theoretically sufficient for a full CV swing, consistent with the experimental observation in Figure 3.2. However, for $\phi_{Bh} = leV$, which corresponds to Al, $\tau = 10^4$ s, so the carriers will not respond for even very low frequencies. The same trend has been observed in experiments-no accumulation behavior has been observed with devices with Al electrode (Figure 3.2). In fact, Figure 3.6 can also be used to explain the trends in the depletion regime (positive gate bias in Figure 3.2). As already mentioned, the thermal generation rates are too low for any significant carrier build up (either electrons or holes). With Au as contact, the barrier height for electrons is now $\phi_{Be} \sim 2.4$, while for Al electrode, the injection barrier is around $\phi_{Be} \sim 1.4$. As evident from the figure, the response time is astronomically large for such electrodes and is among the reasons why no inversion regime is observed in such devices (see Figure 3.2) [30]. We note that the same argument also supports the fact that inversion regime can be obtained with Calcium electrodes ($\phi_{Be} = 0$).

This discussion provides a theoretical background for the role of contacts in the determination of capacitance voltage characteristics. A hypothesis based on the injection of carriers can be used be to explain the CV results and the validity of the concept of

unintentional doping can be argued. To test this hypothesis, we have resorted to detailed numerical simulations, as described in the next section.

3.4.2. Numerical Simulations

The dynamic CV characteristics of the MIS pentacene device were simulated through self-consistent solutions of drift-diffusion equations for carrier transport and Poisson equation for electrostatics. Simulations have been done using a commercial tool Sentaurus provided by Synopsis[®][31]. The capacitance has been estimated from the imaginary part of the complex admittance of the device, which has been numerically calculated by applying a small signal AC bias superimposed on a DC bias [9, 31]. The MIS structure simulated was similar to the one shown in of Figure 3.1, with the exception that the highly doped silicon substrate was replaced directly with back contact Al. This reduced numerical complexity and is well justified since the experimental results in Figure 3.1 show negligible effects of silicon substrate depletion on CV characteristics. The organic semiconductor was treated as intrinsic with a constant trap-assisted thermal generation/recombination rate ($\tau = 1 \ \mu s$). The charge transport is assumed to be band type (similar to MTR model) and constant mobility ($\mu = 0.1$ cm^2/Vs) is assumed in our simulations. For simplicity, the effects due to trap states, grain boundaries and such others have been neglected. The objective was not to fit the experimental data rather to understand and illustrate the crucial role of contact injection on the CV of thin film organic devices. It should be noted that the typically reported value of the dielectric constant 3.6 has been used in the simulations, so that, our results could be compared with the experimental trends reported in literature.

As discussed earlier, the metal organic semiconductor boundary condition is very critical for organic device simulations. Here, we have used the appropriate Schottky boundary conditions to account for carrier injection (assuming thermionic emission) at the top contact [32]. In this approach, the hole density at the top contact/semiconductor interface is given by Eq. (3.5) and the corresponding electron density is given by the following equation Eq. (3.6)

$$p_0 = N_V \exp(-q\phi_{Bh} / kT) \tag{3.5}$$

$$n_0 = N_C \exp(-E_g + q\phi_{Bh} / kT)$$
(3.6)

where E_g is the band gap, and N_C is the conduction band effective density of states. The material parameters used for the simulations have been given in Table 3.1 and correspond to pentacene [11, 33].

 Table 3.1 Simulation parameters used for Pentacene

N _c , N _v	1×10^{20} cm ⁻³
Dielectric Constant	3.6
Band Gap	2.4 eV
Electron Affinity	2.8 eV
Pentacene Thickness	60 nm
Area	$1.26 \times 10^{-3} \text{ cm}^2$

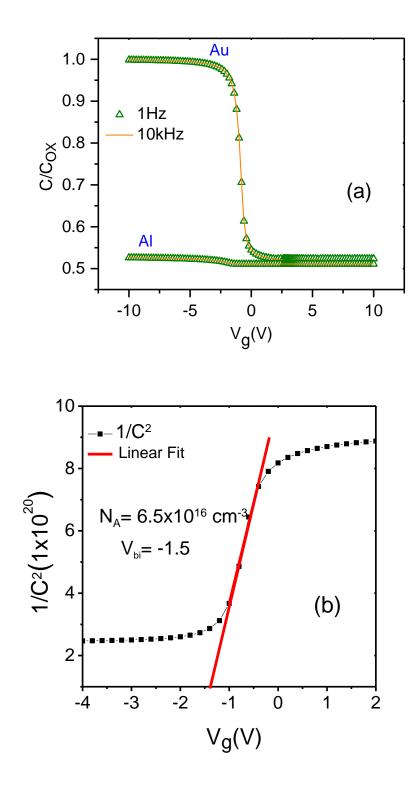


Figure 3.7 (a) Simulated capacitance voltage curve of the undoped Pentacene MIS structure with Schottky top contacts. The two cases shown correspond to the Au ($\phi_{Bh} = 0$ eV) and Al ($\phi_{Bh} = 1 \text{ eV}$) injection barrier. For the two barriers, 1 Hz and 10 kHz did show a significant variation in simulations. (b) Mott-Schottky analysis of Au characteristics to extract N_A and V_{bi}

Figure 3.7a shows dynamic CV results for intrinsic pentacene with Au contact ($\phi_{Bh} = 0$ eV). Remarkably, the simulation results hold a strong similarity to the experimentally observed CV curves of Figure 3.2. Figure 3.7b also exhibits a voltage region with strict $1/C^2$ -V dependence. On application of the Mott-Schottky analysis, the extracted doping density is $N_A = 6.5 \times 10^{16} \text{ cm}^{-3}$ and $V_{bi} = -1.7 \text{ V}$. These values are surprisingly close to the extracted values in Figure 3.3, even when no explicit attempts were made to match the CV characteristics. However, note that, these values do not have any physical significance because intrinsic pentacene was assumed for simulations, while Mott-Schottky analysis was derived for doped semiconductors [9]. Further, the carrier density profile for various bias conditions is shown in Figure 3.8. The carrier density at Au-pentacene interface was given by boundary condition (Eq. (3.5) and Table 3.1), while, it strongly varies with the voltage along the thickness of the pentacene. For positive biases, the semiconductor, except for the thin region near the Au contact, is devoid of any significant charges-both mobile carriers as well as ionized dopants, therefore, the capacitance is given by C_{min} (Eq. (3.4)). As the voltage is increased to more negative values, an accumulation of charges occurs near the oxide pentacene interface. This accumulation charge is entirely due to the contact injection and completely shields the electric field due to applied voltage. Hence, the capacitance saturates at large negative biases to C_{max} (Eq. (3.3)). For the first time, our results, Figure 3.7 and Figure 3.8, demonstrate that CV of thin film organic devices could be contact injection limited and provide an alternative coherent explanation based on injected carriers.

Finally, we address the ambiguity regarding thickness dependent doping densities reported in literature [11, 26, 34-37]. Using simulations, we extracted doping density (through MS analysis of simulated CV results) for intrinsic pentacene devices, as a function of OSC thickness with all the parameters being same as in Table 3.1. The extracted doping densities are shown in Figure 3.9, where the solid line with open symbols indicates simulation results and solid symbols represent experimental data reported in literature (that is, obtained through the MS analysis). Surprisingly, we find that the reported experimental trends follow our simulation results, thus, providing additional independent experimental support to the main theme of this manuscript—extracted "unintentional doping density" could be an analytical artifact of MS analysis, and as such, does not correspond to ionized dopants. Further, as expected, our results indicate that the extracted doping density is indeed independent of pentacene thickness in the presence of an actual doping density should be supported by a corresponding thickness dependent study. If the reported unintentional doping density is real

and not an artifact, one should expect that this result is thickness independent. Figure 3.9 clearly shows that the wide variation in reported unintentional doping densities in literature can be interpreted in a single, unifying framework of contact dominated CV characteristics, as proposed in this work.

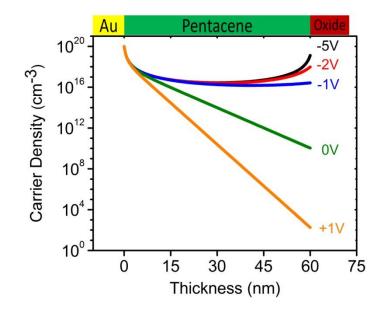


Figure 3.8 Carrier density profile along the thickness of the pentacene. At gold pentacene contact carrier density is fixed by the boundary condition of Eq. (3.5), and at the pentacene oxide interface, an accumulation of charges occurs as the negative bias on the gate increases.

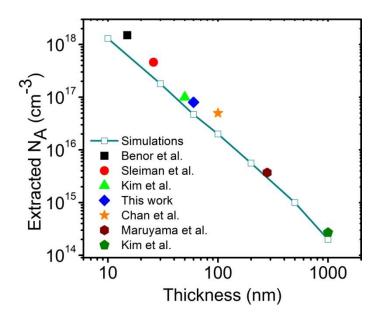


Figure 3.9 Extracted doping density (N_A) as a function of OSC thickness compared with experimental results reported in literature [11, 26, 34-37].

3.5. Estimation of Injection Barrier

3.5.1. Frequency dependent characteristics

The discussion above establishes the role of the injection barrier in determining CV characteristics. An alternative perspective based on the conductivity of a sample, where the carrier density inside the pentacene is determined by the injection barrier can provide a method to extract the injection barrier. In order to verify this theory, we have further characterized the previously discussed atmosphere-exposed pentacene devices for frequency measurements.

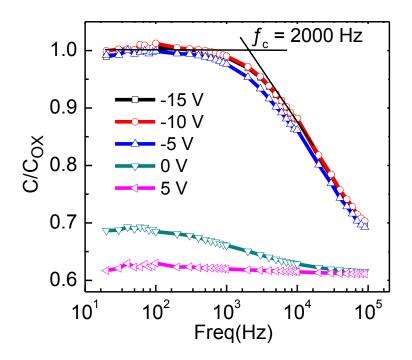


Figure 3.10 Capacitance versus frequency response of atmosphere exposed devices. The cut-off frequency (f_c) is extracted to 2000 Hz.

Figure 3.10 shows the measured frequency response of the exposed sample at different voltages. In the accumulation region (negative biases), the capacitance is strongly frequency-dependent; whereas, in reverse bias (positive bias), it is independent of frequency in the measured range. The injected charges in accumulation are able to respond till the cut-off frequency (f_c) of 2000 Hz. Beyond f_c , the charges are not able to respond with increase in frequency, leading to degradation in capacitance[38].

An insight into the frequency measurement above can be obtained from the relaxation (response) time of the majority carriers [38]. CV is measured from the dynamic response of carriers to the small signal AC bias superimposed on the DC voltage. The majority charge carriers will follow the AC gate voltage as long as the period of the AC voltage (applied frequency) is longer than the dielectric relaxation time (cut-off frequency), Eq.(3.7).

$$\omega \tau >> 1$$
 (3.7)

here ω is the applied AC frequency in radians per second and τ is carrier relaxation time. The carrier relaxation time (τ) depends on the conductivity (σ), given by Eq.(3.8), where *p* is the carrier density and μ is mobility [38].

$$\tau = \frac{\varepsilon_s}{\sigma} = \frac{\varepsilon_s}{q\mu p} \tag{3.8}$$

While the Eq. (3.7) holds, the saturated capacitance corresponds to the oxide thickness; else the capacitance will be attenuated due to the laggard response of the carriers. The response time of carriers also depends on other factors like recombination-generation but is neglected in this study as a first order approximation.

In OSCs, due to a high band gap (> 2 eV), the carrier density is primarily dependent on the injection from the contact. An approximate equilibrium value of carrier density can be estimated using Eq. (3.5) [32]. When Eq.(3.5) and Eq.(3.8) are combined, the response time of the injected carriers will be

$$\tau = \frac{\varepsilon_s \exp(q\phi_{Bh} / kT)}{q\mu N_V} \tag{3.9}$$

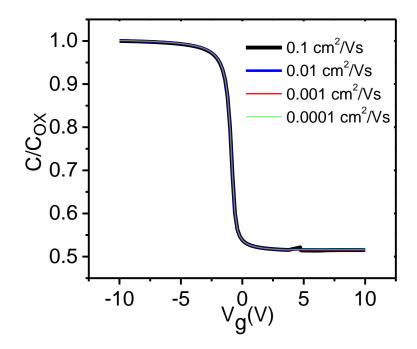
Using Eq. (3.9) for the limiting case of Eq. (3.7), the extracted injection barrier is 0.51 eV for $f_c = 2000$ Hz with an average mobility of 0.1 cm^2/Vs , along with other parameters from Table 1. As will be shown later, the extracted injection barrier is not strongly dependent on the value of the mobility used. The estimated ϕ_{Bh} is surprisingly close to the reported values of the injection barrier from photoelectron spectroscopic studies of ambient-exposed devices[39, 40].

Photoelectron spectroscopic studies have shown that the pentacene-gold injection barrier is very sensitive to exposure to the atmospheric. The exact mechanism of the impact of atmospheric exposure is not precisely known. However, it is suspected that the adsorbed oxygen and moisture interact with pentacene and gold to change the energy level alignment at the metal organic interface [40]. Its impact is explained with the formation of surface dipoles [39], polarization [41], and the change in metal work function [40]. These factors effectively alter the hole injection barrier by $0.4-0.6 \ eV$ [39-41] at the Au/pentacene interface—also observed in our CV measurements.

3.5.2. Numerical Simulations

The model presented above is based on the strong relationship between f_c and the ϕ_{Bh} . While it is known that f_c is also related to the mobility (Eq. (3)) it is of importance to study the relative dependence of the two factors on f_c . Consequently, two dimensional (2D) numerical simulations were carried out to study the relative dependence of the two parameters on capacitance and the cut-off frequency.

Figure 3.11a, the injection barrier was fixed at a low value, $\phi_{Bh} = 0 \ eV$, and the mobility was varied from $0.1 \ cm^2/Vs$ to $10^{-4} cm^2/Vs$. At an applied frequency of $10 \ kHz$, all the CV curves overlapped perfectly, showing no change with the mobility as low as $10^{-4} \ cm^2/Vs$. In the next set of simulations, Figure 3.11b, ϕ_{Bh} was changed from low to a higher injection barrier, keeping the mobility fixed at a value $0.1 \ cm^2/Vs$. The low injection barrier ($0-0.4 \ eV$) did not show any dispersion for 10 kHz. At $\phi_{Bh} = 0.5 \ eV$, a dispersion of $0.9 \ C_{ox}$ is observed, which increases rapidly with further increase of ϕ_{Bh} . Another important point, shown in the inset of Figure 3.11b, is the voltage at which the C_{min} is reached. As observed experimentally, in Figure 3.4. The CV shifts to the left, which is qualitatively similar to the simulations. Here, the CV shifts in the negative direction with a higher injection barrier, supporting our interpretation of injection barrier degradation.



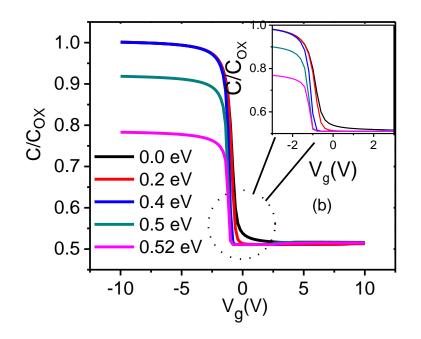


Figure 3.11 Simulation of pentacene based MIS with (a) ϕ_{Bh} is fixed at 0 eV and μ is varied at 10 kHz. (b) μ is fixed at 0.1 cm²/Vs and ϕ_{Bh} is varied at 10 kHz. The inset shows the enlarged CV characteristics around 0 V to indicate the negative shift in CV characteristics with an increasing barrier.

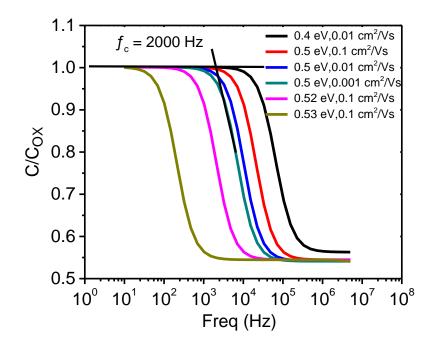


Figure 3.12 Both ϕ_{Bh} and μ is varied and the capacitance is plotted for different frequencies. (ϕ_{Bh} , μ) = (0.53 eV, 0.1 cm²/Vs) resulted in f_c of 2000 Hz.

Further, in a real ambient-exposed device the combination of the ϕ_{Bh} and μ will determine the overall dispersion. Figure 3.12 plots the capacitance versus frequency response for the relevant combination of ϕ_{Bh} and μ . If the injection barrier is very low (0-0.2 eV), the f_c is very high (data not shown) and practically independent of mobility for values reported in pentacene. As the injection barrier is increased to 0.4-0.5 eV, the effect of the mobility becomes more relevant. Since the response time is exponentially related to ϕ_{Bh} , it has a much stronger dependence than the mobility. It is this stronger dependence of the carrier density on capacitance that makes CV an attractive technique. A combination of $(\phi_{Bh}, \mu) = (0.53 \text{ eV}, 0.1 \text{ cm}^2/\text{Vs})$ resulted in a cut-off frequency of 2000 Hz—a close resemblance to experimentally and theoretically calculated values.

3.6. Summary

Finally, in this chapter, we have discussed the capacitance voltage characteristics of pentacene-based metal insulator semiconductor devices. We have highlighted the various anomalies related to the concept of unintentional doping density for organic electronic devices. Historically, the application of MS analysis to organic semiconductors and the over-

sensitivity of OSCs to the environment had led to the idea of unintentional doping. Our results have indicated that unintentional doping density estimated using MS analysis could be an artifact. An alternative explanation for the CV of pentacene devices based on the injection of carriers from the contact electrode has been proposed in this work. It has been shown that CV characteristics of pentacene MIS devices are strongly contact dependent and can be completely explained by the process of contact injection into the undoped OSC. Moreover, our results have indicated that conflicting experimental data from different research groups can be interpreted in a coherent and unified conceptual framework.

Further, atmospheric degradation of pentacene devices has been explained through the degradation of the injection barrier. We have reported that C_{max} dispersion with ambient exposure can be explained by the degradation in the injection barrier. Using a first order timing analysis, a degradation of 0.51 eV has been observed which is close to the reported value (0.4-0.6 eV) from photoelectron spectroscopic studies. The numerical simulations have further proven that degradation is indeed a stronger function of the injection barrier than the mobility. A theoretical model based on the timing analysis has been proposed to extract the injection barrier from the capacitance frequency measurements. Finally, this work has highlighted the fact that many aspects related to fundamental understanding of organic devices need to be revisited in the light of the crucial role of contacts on device performance. Neglecting the effect of the injection barrier can lead to an over estimation of trap density and misinterpretation of other parameters such as doping density, depletion width and flat band capacitance.

3.7. References

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Chapter 4.

Charge Transport in Top Gate Organic Field Effect Transistors

Charge carrier mobility is one of the critical parameters of OFETs. The research on organic semiconductors in the past decade has been focused on the improvement and optimization of their mobility. Factors affecting the mobility could be many—the dielectric interfaces, device geometry, grain size, surface roughness, molecule orientation, doping, strain, and such others. Different research groups have been constantly investigating these factors to understand and improve the performance of OFETs. In this chapter we have studied the charge transport in n-type semiconductors in top gate bottom contact geometry. First we have optimized the morphology for best mobility in top gate structure and, next, used the optimized device to study the effect of bending on charge transport.

4.1. Introduction

The electrical performance of the organic devices is dependent on the mobility of charge carriers inside the organic semiconductors (OSC). Mobility can be measured through different techniques, such as Time of Flight, Hall Effect measurements and the like [1, 2]. These measurement techniques usually require dedicated and complex setups. Besides, relatively, an OSC has very low mobility values, making it difficult for conventional equipment to measure it. The measured mobility in OSCs can be increased using the field effect transistors. Organic semiconductor-based field effect transistors are frequently used to investigate the charge transport in polycrystalline organic thin films.

More than two decades of intensive research in organic semiconductors has led to an unprecedented growth in the performance of organic field effect transistors (OFET) [3, 4]. Different parameters, such as grain size, contact resistance, interface charges and the like, have been shown to be critical to the performance of an OFET. Primarily, three geometries of OFETs have been investigated: bottom gate bottom contact, bottom gate top contact and top gate devices [3]. While the first two structures are well studied, top gate devices are rarely studied due to the complications and limited possibilities with the gate dielectric. The solution processable materials are not possible because the involved solvents would typically cause a degradation of the underlying active layer.

Recently, with advancement in gate dielectric technology, the interest in top gate devices has been revived [5, 6]. Top gate OFETs have a direct technological advantage over bottom gate devices in terms of ease of fabrication and stability because the dielectric layer and the top gate metal electrodes also act as encapsulation layers, which protect the vulnerable organic semiconductor. The deposition of a dielectric from the top is also useful in realizing double gate OFET structures[7, 8]. The interaction at the interface of the dielectric and the organic semiconductor (OSC) is critical to the performance of the OSC. Grain size [9] and surface roughness [10] of the OSC are important parameters and play a critical role in electrical charge transport. Typically, reports have focused on bottom gate devices where the surface roughness of the dielectric is critical since it hinders the electrical transport [10].

In this chapter, we have presented a study of the charge carrier mobility in C_{60} -based top gate OFETs with parylene-C as the gate dielectric. The substrate temperature was varied to get different grain sizes of the C_{60} thin films[11]. Electrical and morphological

characterizations have revealed that in contrast to bottom gate geometry, mobility doesn't strictly increase with increasing grain size. The surface roughness of the C_{60} film also plays a critical role, as it forms the interface with the dielectric deposited from the top. A statistical variation in mobility measured across multiple devices was used to optimize the temperature of C_{60} deposition for optimum performance. The optimum devices have later been used to study the effect of curling and bending on the mobility.

4.2. C₆₀ OFETs

 C_{60} is a recently discovered form of carbon which is semiconducting in nature. In a single C_{60} molecule, 60 carbon atoms are located at the vertices of truncated icosahedron with the nearest neighbor Carbon-Carbon distance of *1.44 Å*. Each carbon is sp² hybridized and triangully bonded to three other carbon atoms, as shown in Figure 4.1. Fullerene or Bucky-Ball is the common name of the C_{60} molecule. The electronic structure and charge transport is determined by the π electron cloud system. The energy band gap of C_{60} varies within the range of *1.43-2.35 eV*.

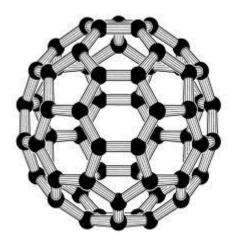
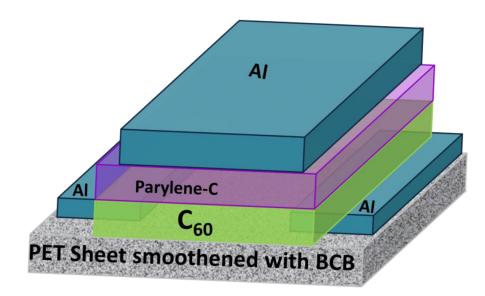


Figure 4.1 Molecular structure of C₆₀

 C_{60} has been lately used in fabrication of various organic devices. Fullerene is an organic semiconductor which shows n-type semiconducting behavior with electrons as majority charge carriers. OFETs made out of C_{60} have shown high mobilities up to 5 cm^2/Vs . Bottom gate OFETs are, mostly, used for fabrication of C_{60} based OFETs [12, 13]. Due to n-type semiconducting behavior of C_{60} , usually low work function metals such as Al are used as

source/drain contact metals to achieve ohmic contacts. A thin layer of LiF is often used to reduce the contact resistance.

Although, C_{60} devices have shown promise in terms of their high mobility, C_{60} devices suffer from fast degradation in atmosphere. C_{60} devices when measured in glove box show long term stability, which proves its potential in electronic application if properly encapsulated. In comparison to bottom gate devices, top gate devices offer an additional advantage in term fabrication simplicity. In top gate OFETs dielectric is deposited from on top of the organic semiconductor which act as both dielectric and encapsulation layer. Figure 4.2 shows the device schematic of a top gate organic field effect transistor that was fabricated during this study.



2.1.2. Fabrication of Top gate OFETs

Figure 4.2 Schematic of top gate C_{60} based organic field effect transistor fabricated on a flexible substrate with parylene acting as both the gate dielectric and the encapsulation layer

 C_{60} OFETs were fabricated on 170-µm thick polyethylene terephthalate (PET) flexible substrates. Atomic force microscopy (AFM) of PET sheets is shown in Figure 4.3a with measured root mean square (rms) surface roughness of 20 nm. The surface of the PET shows a number of non-uniformities, rendering it unusable for OFET application. Divinyltetramethyl disiloxane-bis(benzocyclobutene) (BCB), with the thickness of $l\mu m$ was spun—coated as a smoothing layer reducing the surface roughness to 0.3 nm. The smoother surface provides a uniform growth condition and better adhesion of C_{60} films to the surface. Figure 4.3b shows the improved AFM image of the PET substrate after smoothening. Next, a 70 nm Al source, drain was evaporated through a shadow mask with $W/L = 1800 \ \mu m / 70 \ \mu m$. The PET substrates were next transferred to the chamber of Hot Wall Epitaxy (HWE). C₆₀ deposition is done in a hot-wall reactor where the source material is evaporated in a quartz tube at 360 °C. The upper end of the quartz tube (wall) is heated to 400 °C assuring that the material is only deposited on the substrate, which is placed on top of the tube to form a lid. The substrate is heated to 150 °C in order to increase the mobility of the impinging molecules on the sample surface and therefore reach a higher crystallinity of the C₆₀ film as compared to deposition at room temperature. The pressure in the chamber during the deposition was 1.5×10^{-6} mbar. The deposited thickness of C₆₀ films was 300 nm. HWE has been previously reported to produce high quality crystalline C₆₀ films [11] [9].

Parylene-C of $1 \ \mu m$ thickness was deposited as a gate dielectric. Parylene was deposited using a homemade setup by the method of pyrolysis. Figure 4.4 shows the three-steps of pyrolysis for the parylene-C deposition. The dimer was heated in vacuum conditions at 100 °C. The vaporized fumes were passed through a high temperature zone of 700 °C which cleaves the dimer into the monomeric form. The monomer was finally deposited on to the substrate at room temperature in the polymeric form. The process is carried out at a pressure of 1 x 10⁻² mbar and the growth is monitored in situ via a quartz balance. Parylene has been previously used as a gate dielectric in OFET applications. Its usability as an encapsulation layer has also been tested for various applications. For our top gate devices, using parylene-C as the gate dielectric, we have reduced the processing step and exploited the two known usability of parylene.

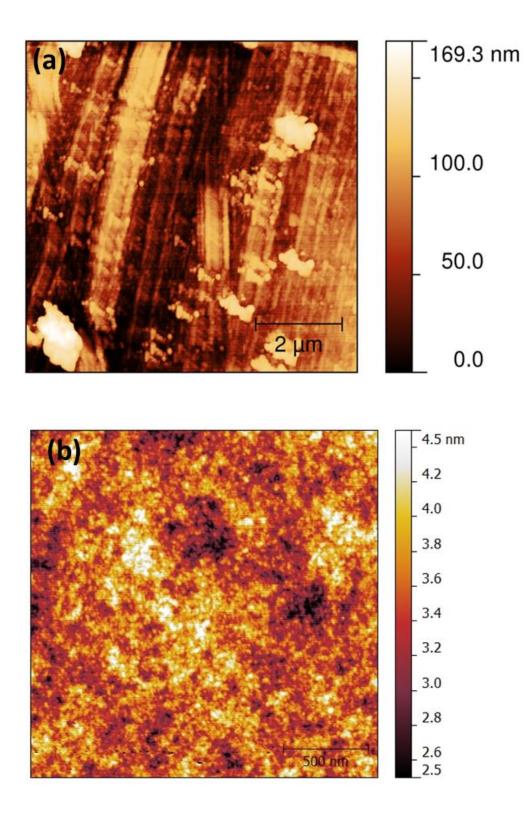


Figure 4.3 AFM images of (a) PET sheet (b) PET sheet smoothened with BCB layer

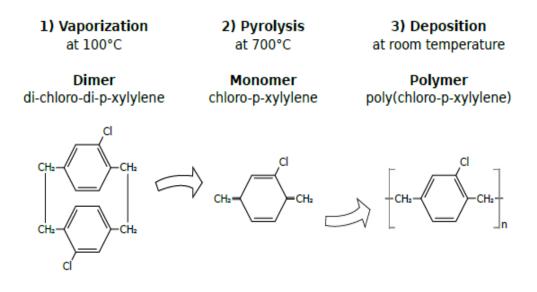


Figure 4.4 Three step deposition process for Parlyene-C film preparation

Finally to complete the device 70 nm of Al gate was evaporated. The top gate C_{60} OFETs exhibited low leakage and high performance with no hysteresis. Electrical characterization was performed at room temperature, in the dark, in a glove box with a nitrogen atmosphere using an Agilent E5273A 2-channel-source unit. Figure 4.5(a) and (b) show the representative output and the transfer characteristics of the device under consideration. The OFET shows a proper transistor swing from the Off state to the On state. The different extracted device parameters given in Figure 4.5b. are

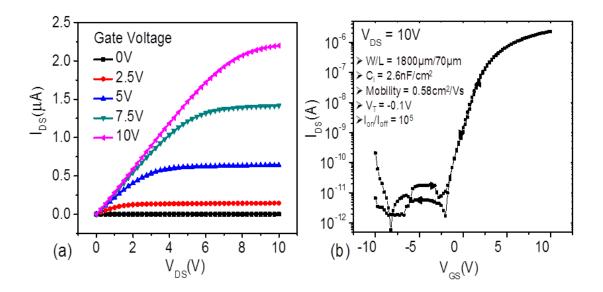


Figure 4.5 (a) I_{DS} - V_{DS} (b) I_{DS} - V_{GS} output and transfer characteristics, respectively, of high performance C_{60} based flexible top gate OFET.

4.3. Mobility Study

3.3.3. Surface Characterization

T _{Substrate}	Grain Size	Surface RMS
	(nm)	roughness (nm)
100 °C	55	4.43
150 °C	75	7.41
200 °C	83	8.64

Table 4.1 Morphological parameters obtained from AFM images

 C_{60} films were deposited using the HWE (please see Appendix C) technique [14] at three different substrate temperatures of 100 °C, 150 °C, and 200 °C. The substrate temperature was varied to get different grain sizes of the C_{60} thin films [11]. The surfaces of the three films were characterized by AFM; the images are shown in the Figure 4.6. AFM studies of the deposited organic films were performed using a Digital Instruments Dimension 3100 in the tapping mode. Surface roughness and grain size of C_{60} films were calculated using the software Gwyddion [15] and are shown in Table 4.1. The grain size increases with an increasing substrate temperature. From 100 °C to 150 °C, the increase in grain size is prominently visible but from 150 °C to 200 °C the increase is relatively small. Along with the increase in grain size, there was also an increase in the surface roughness compared to films prepared at 100 °C. It has to be stated that the surface of C_{60} surface is of prime importance in top gate transistors because it forms the active interface with the dielectric. The polycrystalline nature of the films grown the by HWE technique was also ensured by XRD measurements [16].

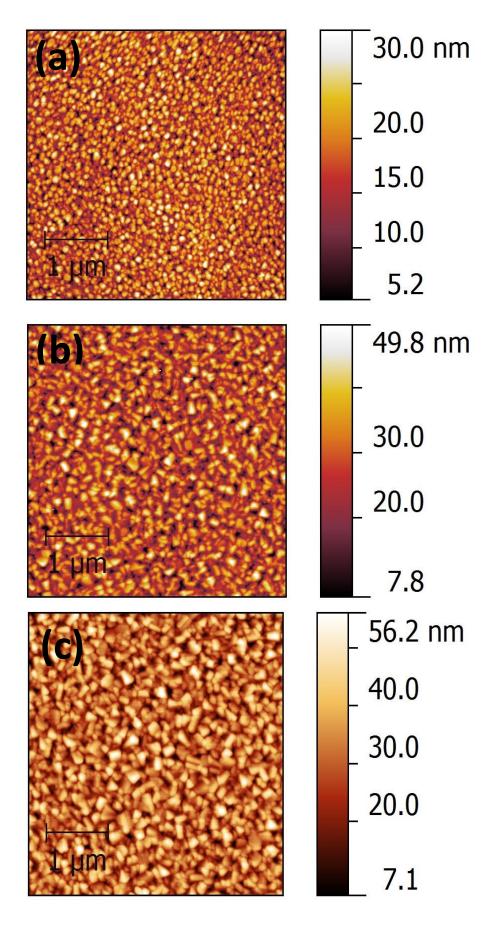


Figure 4.6 AFM images of the C_{60} films was performed at substrate temperatures of b) 100 °C, c) 150 °C and d) 200 °C.

3.3.4. Electrical Characterization

Up to twelve OFETs were fabricated at each substrate temperature to study the statistical behavior of device parameters with the changing morphology of C_{60} films. Figure 4.7 shows representative transfer characteristics of the OFETs deposited at 100 °C, 150 °C and 200 °C of the substrate temperature, respectively. All prepared devices (grown at different temperatures) exhibited high performance, showed low leakage (in the order of 10^{-10} A), a high on-off ratio and an almost negligible hysteresis.

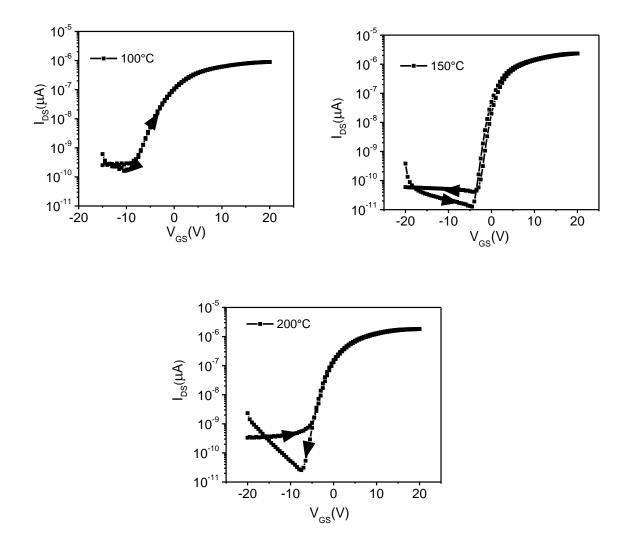


Figure 4.7 I_{DS} -V_{GS} characteristics of the OFETs deposited at 100 °C, 150 °C, and 200 °C, respectively.

Figure 4.8 shows the statistical distribution of mobility for the best five devices at each substrate temperature. The charge carrier mobility of the devices is extracted from $\sqrt{I_{DS}}$ versus V_{GS} curves. The mobility shows a nonlinear trend with increasing substrate temperature, which is in contrast with the bottom gate devices where the mobility increases with an increasing grain size [9, 11]. The mobility is lowest for the OFET that is grown at a temperature of 200 °C and the maximum for the one grown at 150 °C. Although the grain size shows an increasing trend with the substrate temperature, the mobility does not increase further.

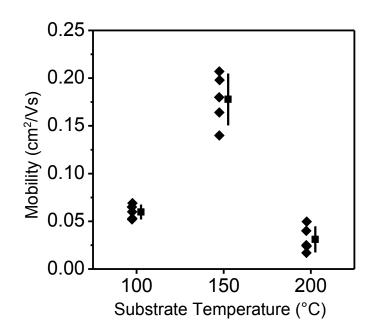


Figure 4.8 Statistical variation of mobility measured in five devices versus the changing substrate temperature. The mean value and the standard deviation are plotted next to the data points.

These results can be explained in terms of surface roughness. In bottom gate devices, the dielectric surface provided both the growth surface and the insulator semiconductor interface. However, for top gate, the smoothening layer of the BCB provided a high quality growth condition; whereas, the C_{60} surface formed the active interface with the parylene dielectric, making its roughness critical to the overall charge transport. In Table 4.1, the surface roughness is reported to increase with increasing substrate temperature. At 100 °C the grain size is critically small—limiting the mobility. At 200 °C, the grain size has increased but the surface roughness is almost twice as high as the samples grown at 100 °C. As a result,

 C_{60} forms a bad interface with parylene leading to a lot of trap states and surface scattering, subverting the mobility enhancement by the increased grain size. An optimized state is reached for the films grown at 150 °C, where a tradeoff between increasing grain size and surface roughness is achieved.

4.4. Strain Analysis

Mechanical flexibility is one of the key advantages of organic materials in applications such as wearable-electronics or flexible displays [17-19]. It is consequently important to understand the effect of strain on these materials due to rolling, twisting and curling of large flexible substrates for a variety of applications. Curling of a flexible substrate has been known to introduce strain in organic devices [18, 20]. In silicon-based integrated circuit applications, strain effects play a significant role in improving the device performance and considerable insight has also been gained in the role of strain in charge carrier transport [21]. In silicon, the effect of strain on p-type and n-type devices is complementary. It is reported that in silicon under compressive strain, the hole mobility in p-type devices increases, whereas, the electron mobility in n-type devices decreases. With tensile strain, the effect on carrier mobility for nand p-type silicon devices are opposite in nature [21, 22]. Although silicon is crystalline and organic semiconductors (OSC) are polycrystalline, and the impact of strain could be significantly different, it is interesting to compare the effect of strain in p-type and n-type OSC materials. The effect of strain in p-type OSC-like Pentacene was explored in detail by Sekitani et al. [20] and Jedaa et al. [23]. It has been reported that on application of compressive strain, mobility increases and under tensile strain, it decreases. Furthermore there have been reports where strain is studied from in the aspect of reliability assessment and degradation, where organic circuits are monitored with the application of strain to identify the bending limits of flexible devices [24]. However, no systematic studies on the effect of strain on n-type OSCs have been reported in literature, which is the focus of this work. We have fabricated high mobility, flexible top gate C₆₀ transistors and systematically investigated the effect of bending on electronic charge-carrier transport.

4.4.1. Experimental Details



Figure 4.9 Schematic of the clamp holding the substrate

Strain on the organic semiconductor was applied by curling the PET substrates on which the devices are fabricated. Flexible substrates were mounted between the clamps and the devices were curled by the translational motion of the clamps, as shown in Figure 4.9. The strain incurred by the organic semiconductor can be approximated with the strain experienced at the surface of the substrate. At a bending radius *R*, the strain on the substrate surface $\varepsilon_{surface}$ can be expressed using the Eq. (12.1) [25]

$$\varepsilon_{surface} = \left(\frac{d_f + d_s}{2R}\right) \frac{(1 + 2\eta + \chi \eta^2)}{(1 + \eta)(1 + \chi \eta)}$$
(4.1)

where d_f is the film thickness, d_s is the substrate thickness, and

$$\eta = d_f / d_s \quad , \tag{4.2}$$

$$\chi = Y_f / Y_s \tag{4.3}$$

and Y_f , Y_s are Young's moduli of the film and the substrate, respectively. The d_s and d_f are 170 μm and ~1.5 μm , respectively. η could be estimated as 0.01. Further, Youngs modulus of organic materials usually ranges from 0.1 *GPa* to 10 *GPa* [26]. It is safe to assume that the

 Y_f will be less than Y_s as it is a polycrystalline film. Hence, χ would be very less. Therefore Eq (4.1) can be approximated as

$$\varepsilon_{surface} = \frac{d_f}{2R} \tag{4.4}$$

The radius of the curvature of the flexible substrates was extracted by fitting the cross sectional optical image using the software Corel Draw[®]. The substrates were curled between the bending radii of *15 mm* and *5.1 mm* and the corresponding strain was calculated using Eq. (4.4). The devices were measured in four configurations with applied strain (compressive or tensile) parallel and perpendicular to the direction of source-drain current in OFETs. Figure 4.10 (a-d) shows the four measured configurations.

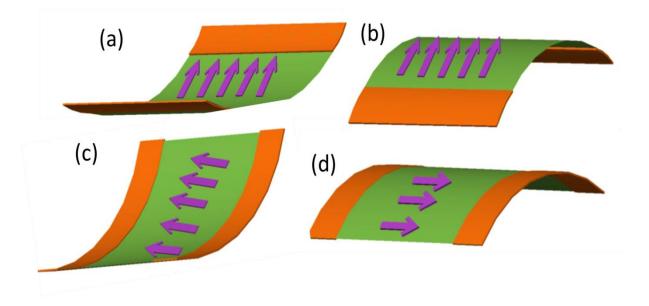


Figure 4.10 (a) - (d) shows four configurations with current parallel and perpendicular to compressive strain (a),(c) and tensile strain (b)(d).

4.4.2. Results

In the first set of experiments we applied compressive and tensile strain and measured current and voltage, parallel to the direction of applied strain. Figure 4.11 shows the corresponding transfer characteristics. Initially, we measured the device at flat conditions and then reduced the bending radius (15 mm > R > 5.1 mm) in a concave (compressive) direction.

We then measured the device again in a flat condition before bending it in a convex (tensile) direction. The saturation current increases with increasing compressive strain and decreases with increasing tensile strain. For a bending radius of *5.1 mm*, the saturation current increases by 80% and decreases by 70% for compressive and tensile strains, respectively; that represents a major change in current levels. This change was found to be reversible after compressive strain but tensile strain caused a reduction in drain current by 65% after the first trail.

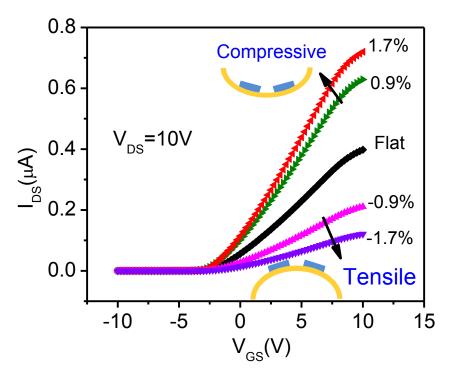


Figure 4.11 Transfer characteristics I_{DS} - V_{GS} when current is parallel to applied compressive and tensile strain. Inset gives the corresponding applied strain values and schematic of the translation stage

To analyze the electron transport under strain condition further, we fabricated another set of devices with similar characteristics and measured the current with the strain in direction perpendicular to the source-drain current. A negligible change was observed in the saturation current in the cases of compressive and tensile strain. The charge carrier mobility (μ) was extracted from the slope of $\sqrt{t_{DS}}$ versus v_{GS} plot. In Figure 4.12 the change of electron mobility versus strain for both sets of experiments is depicted. Mobility monotonically increases (decreases) when the compressive (tensile) strain is applied parallel to the direction of the charge transport; however, it is almost constant for the perpendicular case. Mobility increased from 0.11 cm^2/Vs to 0.22 cm^2/Vs , which is more than a 100% increase for 1.7% of compressive strain. This points towards the potential of C₆₀ to be used in low cost stress sensor applications [27]. The gate leakage of the devices was independent of strain, which highlights the stability of parylene-C as a gate dielectric for bending applications.

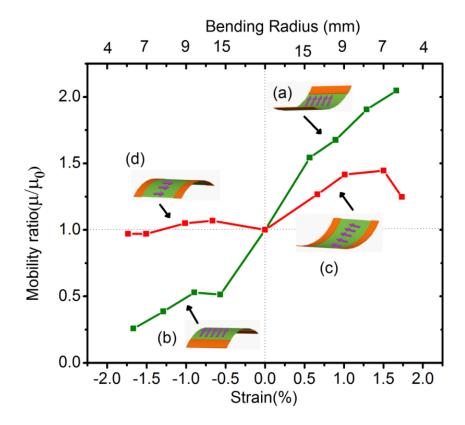


Figure 4.12 Mobility versus strain for a bending radii of R where (15mm > R > 5.1mm). The green and red curves correspond to parallel and perpendicular measurements respectively. The inset shows four curling configurations pointing to mobility measurements in those states. Purple arrows depict the electron transport directions. Current parallel to (a) compressive and (b) tensile strain and current perpendicular to (c) compressive and (d) tensile strain. Mobility change with strain is more prominent for strain parallel transport to the transport than the perpendicular

The observed effect of compressive and tensile strain on electron transport in C_{60} films is qualitatively similar to that observed for p-type OSC-like pentacene [20, 23, 27]. However, as our results have shown, the change in mobility for C_{60} -based devices is almost one order of magnitude stronger than that reported for pentacene [20, 23]. This may be due to the fact that our devices are top gate transistors where the dielectric layer acts as an encapsulation layer. The top encapsulation layer supports the performance of the device. It reduces the probability of grains being dislocated and ensures a homogenous distribution of force in the OSC layer.

4.4.3. Simulation

A remarkable result of this study is that the strain effect on the mobility in C₆₀-based OFETs is found to be strongly anisotropic with respect to the direction of applied strain. This observation is in variance to earlier observations by other research groups in pentacene OFETs where the change in source-drain current did not depend on the direction of the strain relative to the direction of the current flow [20]. The change of μ upon compressive or tensile strain can, in principle, be either due to the change of the intermolecular distances affecting the overlap between neighboring sites or/and due to the change of the energy distribution of localized sites (energetic disorder) in the film. It is worth noting that an increase in conductivity under the applied pressure has been demonstrated in OSC films long ago [28] and was attributed to the enhanced intermolecular coupling in films. Applied strain could also change the energy of localized states (traps) controlling the charge carrier mobility; this is because, in a non-polar material such as C_{60} , the electronic polarization energy is mainly determined by intermolecular distances [28]. However, the creation of deeper localized states (or traps) will only be determined by the stress magnitude and should not depend on the applied stress direction. Thus, the observed strong anisotropy of the strain effect implies that the change in the charge mobility in C_{60} films is mostly dominated by the intermolecular coupling factor rather than the energy distribution of traps; thus, it can discriminate between these factors.

To get a deeper insight into the origin of the observed strain effect on the charge carrier mobility, we fitted our experimental data by the Fishchuk analytic Extended Gaussian Disorder (EGD) model for OFET mobility [29, 30] this model has been recently used to describe temperature activated and electric-field dependent OFET mobility in C₆₀ films [30]. All material parameters used were the same as for bottom-gate C₆₀ OFET studied before [29, 30] and only the hopping distance between neighboring sites, *a*, was varied to get the best fit with the experimental data. For films in flat condition we used a=1.4 nm (intermolecular distance in C₆₀ crystal [31]) as a representative value for such films. The parameter *a* affects, mostly, the mobility prefactor, the position of the effective transport energy level and the electric-field dependence term (see Ref. [30] for details). Mobilities calculated according to Ref. [30] as a function of intermolecular distance are presented in Figure 4.13 (solid red curve) and demonstrate an excellent agreement with the experimental data (symbols) on the strain dependence of μ . Similar fitting results were also obtained by the Pasveer/Coehoorn EGD model [32] using the same set of material parameters (solid blue curve in Figure 4.13).

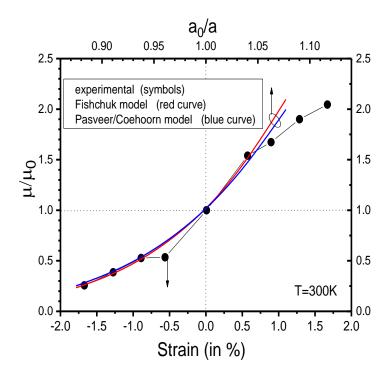


Figure 4.13 The best theoretical fit of the electron mobility data (symbols) measured at different strains applied along the current flow direction by the Fishchuk model (solid red curve) and by the Pasveer/Coehoorn model (solid blue curve). Parameters used for calculations of μ versus *a* intermolecular distances are: $a_0 = 1.4 \text{ nm}$, $a_0/b = 5$ (where b is the electron localization radius), the width of the DOS $\sigma = 85 \text{ meV}$, and the carrier concentration in OFET channel $n/N = 10^{-3}$.

An essential conclusion that can be drawn from the comparison of experimental results and modeling is that in order to explain the observed twofold increase (decrease) of μ upon applied 1.7% compressive (tensile) strain in C₆₀ films, one has to assume a relative decrease (increase) in the intermolecular distance to be as large as ~10%. The latter is clearly impossible for the 1.7% strain because even for ideal adhesion between the substrate and C₆₀ films, the change of the intermolecular distance under such a condition is expected be of the order of 1–2% only.

4.4.4. Analysis

To solve the puzzle, it has to be taken into account that thin films of C_{60} have a polycrystalline [11] morphology with a number of grains and grain boundaries. Grain

boundaries form the weakest link in organic thin films in term of mechanical deformation; it is, therefore, logical to assume that the majority of applied strain will be mostly absorbed at the grain boundaries. When strain is applied, these grain boundaries tend to get closer or move apart leading to a change in grain boundary resistance [33, 34]. This change in resistance is captured as a change in mobility, as observed in our results. It also explains the anisotropic effect of strain on mobility, as observed in our results. In the case of perpendicular strain, grain boundaries perpendicular to conduction get closer, but have a lesser impact on the transport. This indicates that, for wide area applications, devices fabricated perpendicular to the major axis would give a more reliable performance. Thus, we suggest that relative change of inter-grain distances can be quite considerable and is responsible for the observed strain effect. First, grains are weaker coupled between each other compared to intermolecular coupling within crystallites. Second, it is well-known that charge transport in polycrystalline films is controlled by grain boundaries which create five major potential barriers [34-36] (both traps and scattering centers) between the more ordered domains. Indeed, the mobility activation energy in C₆₀ films was seen to decrease with increasing average grain size [9], accompanied by a drastic enhancement of the electron mobility and the grain boundaries were recently found to determine the electric field dependence of μ in polycrystalline OSC films [35]. As we have demonstrated, [35] the rate limiting charge transfer events are likely to be the intergrain jumps; therefore, the complex charge hopping transport problem in such films could be reduced to considering just the most difficult jumps over the grain boundaries. This is reminiscent of charge transport in a conjugated polymer where the limiting step is the jump between conjugated (more ordered) segments of neighboring chains. The barrier heights due to grain boundaries are subject to distribution over the film. Therefore, taking into account a huge variety of percolative passes between the wide (1.8 mm) source and the drain electrodes of an OFET device, the charge transport in average could be considered as that occurring in an effectively random disordered system even though charge carriers may experience just a few crossings over grain boundaries in a particular percolative pass. Thus, it is plausible that the energy distribution of the charge donating and charge accepting states at the grain boundaries follows a Gaussian distribution. This justifies the application of the Gaussian disorder formalism to consider the average charge mobility in such OFET channels. This idea has been recently verified experimentally for polycrystalline silylethynyl-substituted pentacene films [35] and thereby the EGD model is able to accommodate grain boundaries to describe charge transport in polycrystalline OSC films.

4.5. Summary

In this chapter we have studied top gate bottom contact C_{60} -based organic field effect transistors using a parylene-C as the gate dielectric. The fabrication sequence is advantageous in terms of the reduced number of steps involved in fabricating this structure. The morphology of C_{60} films was varied with the substrate temperature. The change in morphology is both in terms of grain size and surface roughness of C_{60} . With increasing temperature, both grain and surface roughness of C_{60} increases. The parylene films deposited on C_{60} determines the semiconductor and dielectric interface. It is found that the mobility of the top gate devices does not increase with increasing grain size. The increasing surface roughness of C_{60} caused by bigger crystal size at elevated growth temperatures critically influences the overall charge transport of the organic semiconductor.

Further, the optimized OFETs at 150 °C were studied for the strain effect on electron transport. Change in the electron mobility upon applied 1.7% of compressive/tensile strain is found to be relatively large—considerably exceeding values reported before for other OFETs. In contrast to the latter, the strain influence of electron mobility in C_{60} films is strongly anisotropic with respect to the direction of applied strain. The observed anisotropy suggests that the effect is dominated by the change of the effective hopping distance—most probably of jump distances over the grain boundaries which dominate the charge transport in polycrystalline C_{60} films. Furthermore, in roll-to-roll processing, for better strain reliability and sensor applications, the direction of the current should be made parallel or perpendicular to major rolling axis, respectively.

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Chapter 5.

OFETs Operation at Elevated Temperature

Performance and stability are two important factors that need to be optimized for the successful deployment of OFETs. In practical applications, the devices have to work in realistic ambient environments, such as humidity, oxygen and temperature variation. A successful application based on organic devices has to work under these circumstances. In this chapter, we have studied the operational stability of pentacene-based OFETs in air, at elevated temperatures. The chemical, thermal and structural stabilities of pentacene thin films have been investigated and their impact on electrical characteristics has been simultaneously analysed.

5.1. Introduction

Organic Semiconductor-based devices have shown a potential for use in a wide range of niche applications, such as the Radio frequency identity (RFID) tag [1], the backplane transistor matrix of flat panel display [2], and lighting applications [3]; these are either very expensive or impossible to fabricate through conventional silicon technology. As these devices are closer to reality a new problem pertaining to the reliability of organic devices has come to the light. The organic devices operating at high fields and prolonged hours are likely to get heated increasing the operating temperature of the device stack [4, 5]. A large matrix of organic devices will collectively generate heat increasing the operational steady-state temperature to 50–60 °C [4, 5]. Further, the ambient temperature can contribute to excess heating of the device, thus exacerbating the operational temperature requirements. Consideration of these practical limitations and identification of the factors that affect device operability at high temperatures are crucial for successful and durable deployment of organic devices.

There are fewer reports on the characterization of organic field effect transistors (OFET) at elevated temperatures and most of which have concentrated on the impact of annealing [6, 7]. In other works, the stability of OFETs at high temperatures is tested in inert conditions [8] [9]. These works have been limited in their scope with the focus on the charge transport. Studies at high temperatures in organic semiconductors are not only important for understanding the charge transport but also can give insight into the degradation mechanism with temperature in ambient conditions.

In this chapter, we have presented a comprehensive analysis of electrical and material characteristics of pentacene-based devices in the temperature range of 25 °C to 150 °C— measured in ambient conditions. The chemical, thermal and the structural stabilities of pentacene (chemical structure shown in Figure 5.1a) thin films have been investigated and their impact on electrical characteristics have been simultaneously analysed. It has been found that pentacene is stable in hot air environment and its crystallinity is intact up to 150 °C. The stability of the current characteristic in OFETs (device structure is shown in Figure 5.1b) at high temperatures is dependent on the thermal stability of the gate dielectric as well as the interfacial characteristics of the dielectric. The carrier mobility within the stable range of temperature has been found to be temperature-independent in the absence of trap sites. However, the mobility is thermally activated in the presence of interface defects. It has been

demonstrated that Pentacene OFETs work reliably under thermal stress and repeated cycles in the air and do not oxidize or degrade due to thermal mechanical stresses.

5.2. Experimental Details

Pentacene films were characterized by X-ray photoelectron spectroscopy (XPS), X-ray diffraction (XRD) and atomic force microscopy (AFM). The pentacene thin film was deposited on one large substrate. The substrate was cut into two sets, one was used for annealing and the other sample was used, as deposited, for comparison. The films were heated in ambient conditions at different temperatures for one hour before being characterized. XPS studies allow us to quantify the different elemental compositions present in surface of the analyzed film. A surface scan of the pentacene film was carried out using the ULVAC-PHI system (Model: PHI5000VersaProbeII) with an Al anode as the source of the soft X-ray beam. A wide range scan was carried out to detect the presence of all possible elements. A narrow scan for C1s peak was done between the energy range of 275 eV and 290 eV with the step size of 0.08 eV. The change in the crystal orientation of pentacene films due to heat can be analyzed using XRD. The experiment was conducted using high resolution Rigaku system (Model: Smartlab 3KW) with a Cu-K α (λ =1.541Å) X-ray source. The scanning range of 2 θ is 3° to 30° in steps of 0.01°. Morphological imaging of the pentacene surface was carried out in the tapping mode using Veeco NanoScope IV Multi-Mode AFM.

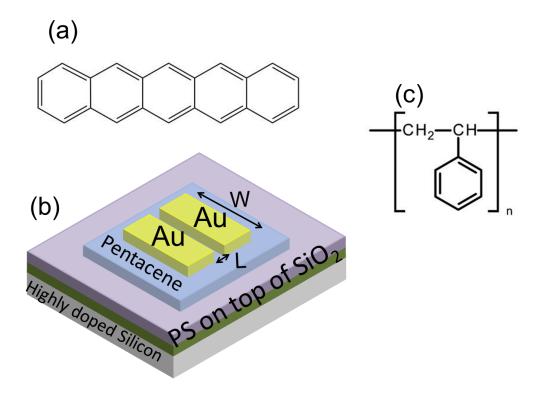


Figure 5.1 (a) Chemical Structure of Pentacene (b) Schematic of bottom gate top contact OFET with PS/oxide as gate dielectric (c) Chemical Structure of Polystyrene (PS)

Pentacene-based OFETs (schematic shown in Figure 5.1b) have been used as a test structure in this work for electrical study. A p-type highly doped silicon wafer was used as a substrate. An oxide of thickness 76 nm was thermally grown on the silicon wafer. The backside oxide of the wafer was etched in a BHF solution. Piranaha cleaning of the wafer was done to further clean the surface and make it hydrophilic. The substrates were heated in a clean environment for half an hour at 120 °C to eliminate the moisture from the surface. We fabricated two sets of OFETs; in the first set, pentacene was deposited directly on the oxide and in the other, the pentacene was deposited on a thin polymeric dielectric layer. A 1% polystyrene (PS-chemical structure shown in Figure 5.1c) solution in toluene was spin coated (2000 rpm) on a piranaha-cleaned oxide wafer. A smooth and pin-holes-free PS film was observed under a high resolution (40x objective lens) optical microscope (Olympus). Pentacene, triple sublimed with 99.9% purity from Sigma Aldrich, was evaporated at room temperature using a shadow mask with a deposition rate of 0.1 nm/s in order to achieve a thickness of 50 nm. Au source/drain contact was deposited using a shadow mask with W/L =700um/70um. After the complete OFET was fabricated, Al was deposited on the back side of the wafer to make a good contact with highly doped silicon. Electrical characterization was done using Keithley® SCS 4200. The devices were heated to a temperature of 190 °C on a Temptonic chuck with an inbuilt heating coil. All characterization was done in dark and

ambient conditions with humidity of 40-50%. The results presented in this study represent a typical dataset measured over multiple samples in different runs.

5.3. Results and Discussion

5.3.1. Chemical Stability

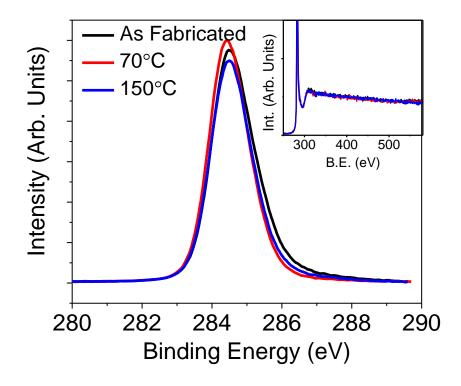


Figure 5.2 A narrow range XPS scan shows almost perfect alignment of C1s peaks observed in as-deposited pentacene samples along with the samples annealed in air at 70 °C and 150 °C. The inset shows a wide range surface scan which shows only the C1s peaks without the presence of any oxygen after heating at 150 °C for 1 hour in air.

In the line of different experiments, foremost is the stability of pentacene thin films in ambient condition at elevated temperature. Ambient stability of pentacene is disputable and as pentacene is often believed to get oxidized in air [7, 10, 11]. Such an oxidation phenomenon is likely to exacerbate at high temperatures. Consequently, first we have studied the chemical

stability of 50 nm pentacene deposited on SiO₂ due to heating under ambient conditions using X-ray photoelectron spectroscopy (XPS). XPS probe core energy levels and provide information about the chemical composition in the pentacene film. As pentacene interacts with ambient moisture and oxygen [12], due to charge transfer, core level binding energies are likely to change [13]. A series of XPS scans of pentacene films were compared to investigate the impact of environmental moisture and oxygen at elevated temperatures, as shown in Figure 5.2. The XPS scan of a freshly prepared pentacene film shows C1s peak at the binding energy (BE) of 284.5 eV, corresponding to the sp² hybridized state of carbon atoms in the pentacene structure similar to previous reports [13, 14]. On heating the samples in ambient air (Relative humidity 50%) for 1 hour at 70 °C and 150 °C, no significant change in the carbon states were observed. Yang et al. have reported different oxidized states of carbon on aging [13]. An attempt to deconvolute HO-C, C=O, HO-C=O peaks around the main C1s peak, did not successfully result in any clear signature of oxidized carbon states as reported for few monolayer thick pentacene film that was exposed to UV light [13]. It implies that these carbon states are not formed in the bulk of the film at temperature as high as 150 °C in ambient conditions. The wide range scans of pentacene shown in the inset of Figure 5.2 do not show the presence O1s states (532 eV) [14]. Although, a few samples did show a small percentage of contaminant oxygen, it was removed by pre-sputter (X-rays energy 2 keV) of 10 seconds. Such contamination of oxygen is limited to the top few nanometers of the surface of pentacene and is unlikely to impact the charge transport that is occurs at the semiconductor dielectric interface [14]. Hence, these XPS results prove the chemical stability of pentacene films at elevated temperatures in ambient conditions.

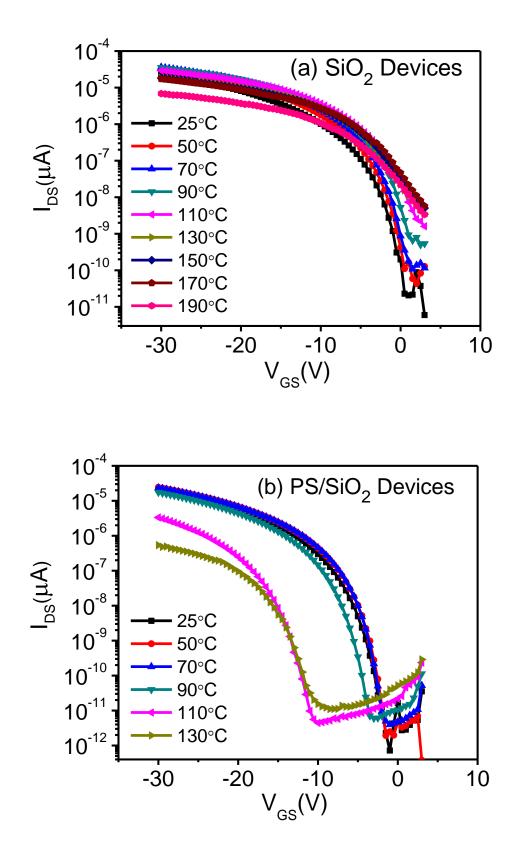


Figure 5.3 Transfer characteristics of OFETs on (a) SiO_2 (b) PS/SiO_2 as a dielectric measured at elevated temperatures in dark ambient conditions

Pentacene based Organic Field Effect Transistors (OFETs) were fabricated to investigate the electrical characteristics at elevated temperatures. Considering the performance variation of OFETs on different dielectrics [15] [16], we have studied the OFETs on SiO₂ and PS spin coated on SiO₂ as the dielectric. We characterized our devices electrically, while the temperature of the OFETs was varied in the range of 25 °C to 190 °C. This was different from previous studies, in which, the devices were annealed at a high temperature but measured at room temperature [11, 17]. Figure 5.3a and b show the representative transfer characteristics of OFETs, measured over the temperature range of 25 °C to 190 °C to 190 °C for the SiO₂ dielectric and 130 °C for PS/SiO₂ devices at $V_{DS} = -30V$. The devices were heated in dark ambient conditions for 15 minutes at each temperature before making the measurements. A well-defined transistor action can be observed in both the devices, over the measured temperature range. The degradation in the On-current (I_{ON}) at 190 °C is attributed to the burning of the contacts. The change in transfer characteristics with the temperature is gradual, with distinct variations in the threshold voltage and the Off-current, with the increasing temperature.

The above-room-temperature range is an intense operating environment for organic devices which are known to have low melting point and low temperature stability. The changes in the current-voltage characteristics at these temperatures can be due to two factors— the alteration in the material properties due to heating or the effect of temperature on the charge transport. These two factors need to be sequentially studied to have in depth understanding of the electrical behavior of OFETs at high temperatures.

5.3.3. Structural and Morphological Studies

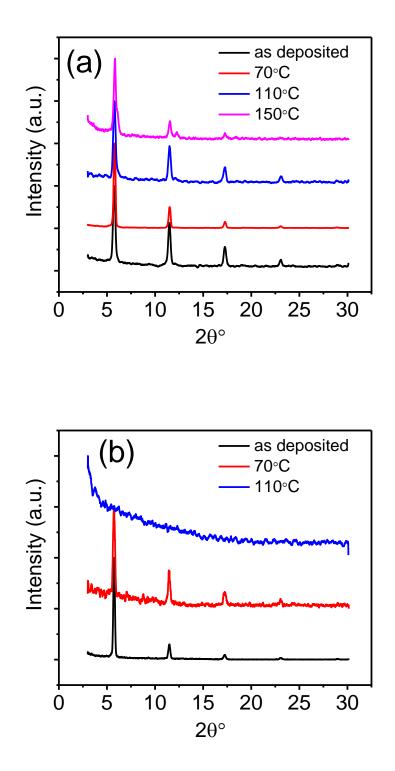


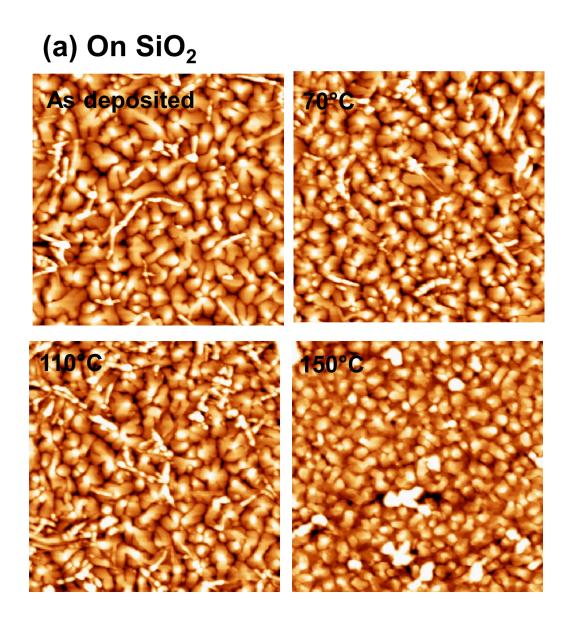
Figure 5.4 XRD of Pentacene films deposited on (a) SiO_2 before and after heating at 70 °C, 110°C, and 150 °C, (b) PS before and after heating at 70 °C and 110 °C

First we have studied the effect of heating on the structural and packing aspects of the polycrystalline domains of pentacene using X-ray diffraction (XRD) and atomic force microscopy (AFM) measurements. Figure 5.4a and 5.4b show the XRD patterns of the pentacene thin film (60 nm) on the oxide and PS/SiO₂ dielectrics, after annealing in air for 1 hour at different temperatures which ranged from 25 °C to 150 °C. We obtained four Bragg reflection peaks in as-deposited pentacene films on both the dielectrics, at 2θ = 5.74°, 11.46°, 17.25° and 23.06°, which can be indexed as (*001*) reflections. These peaks indicated a strong preferential alignment of pentacene molecules parallel to the substrate surface. The following crystal phase can be identified as the "thin film phase" with *d*₀₀₁ spacing of *15.4 Å* with pentacene molecules packed in a layered structure forming a herringbone pattern within the layer [18].

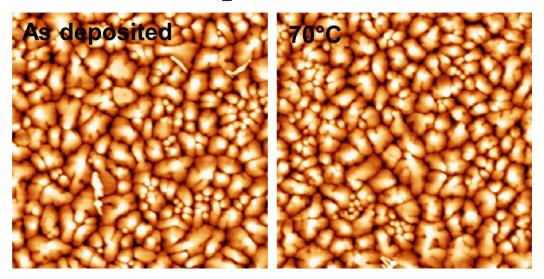
Pentacene molecules are known to arrange themselves in different polymorphic forms, depending on the substrate as well as the processing temperature [19]. The impact of annealing on the crystallinity of pentacene is particularly of interest due to the large anisotropic thermal expansion coefficients in different directions with negative values reported in one direction[20] [21]. The evolution of different phases can be visibly seen through AFM studies. Figure 5.5 shows a series of AFM images of a pentacene thin film taken on SiO₂ (see Figure 5.5a) and PS/SiO₂ (see Figure 5.5b) dielectric substrates at temperatures that range from 25 °C to 150 °C; a similar sample was used for XRD studies. The effect of annealing on the crystallinity of pentacene films at elevated temperatures was comparatively more pronounced on PS substrates. We observed that the crystalline domains of pentacene remained unchanged for up to 70 °C of heat treatment in ambient conditions. On further increase of temperature, the morphological evolution varied distinctively on two substrates.

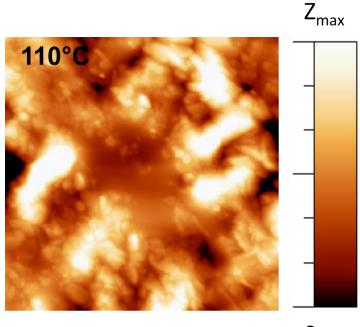
On PS substrates, at 110 °C we observed a complete loss of crystallinity in the pentacene films. An Amorphous pattern in the XRD (Figure 5.4b) and AFM images (Figure 5.5b) can be attributed to the loss in viscoelasticity of the PS film due to heating above its glass transition temperature. The change in viscoelasticity altered the molecular entanglement between the pentacene molecules and the heated PS destroys the crystalline packing of the pentacene molecules [22]. The film deformation at 110 °C led to the formation of island-like structures of uneven heights—explaining the unduly large values of Z_{max} in Figure 5.5b. At the oxide interface, the transformation of pentacene phases was relatively slow with the temperature. There is no perceivable change in crystallinity and morphology of pentacene

films till 150 °C. At around 150 °C, an evolution of another polymorph of pentacene corresponding to d_{001} spacing *14.4 Å*, named as Campbell or "bulk phase" was observed along with the "thin film phase" [20]. This phase change is accompanied by the morphological transformation, seen in AFM images. The grains, after heating at 150 °C, disintegrate into smaller grains with apparently more number of grain boundaries diffusing into each other compared to the AFM images taken at lower temperatures. The irreversible transformation into the bulk phase was due to the higher thermodynamic stability of the pentacene films in the bulk phase compared to the metastable thin film phase [23]. The existence of various polymorphic forms along the direction of the charge transport implies non-uniform molecular π -overlaps, leading to a high trap density and mobility degradation.



(b) On PS/SiO₂





0 nm

Figure 5.5 5 μ m x 5 μ m AFM images of Pentacene films deposited on (a) SiO₂ as deposited and after heating at 70 °C 110 °C and 150 °C (b) PS before and after heating at 70 °C and 110 °C. The values of Z_{max} on oxide are 36 ± 2 nm for all films, except that at 150 °C it is 45 nm. On the PS dielectrics, Z_{max} is equal to 28 ± 2 nm for as deposited films and films heated at 70 °C, whereas, for films heated 110 °C it is 106 nm. Z_{max} is the maximum height on the scale.

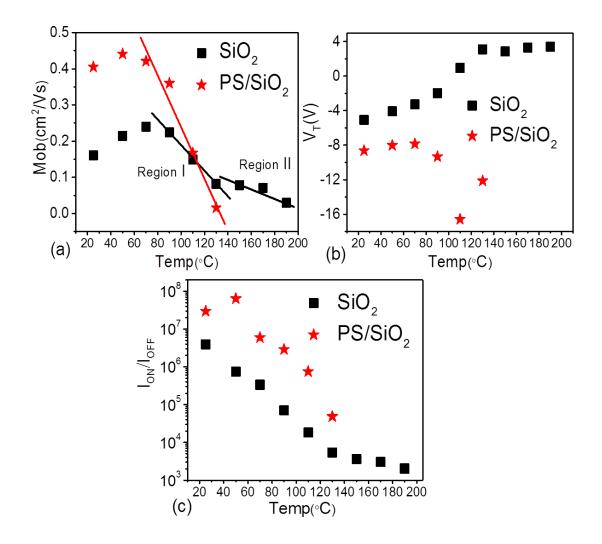


Figure 5.6 Variation in (a) Mobility, (b) Threshold Voltage (c) I_{ON}/I_{OFF} ratio with the temperature for two sets of OFETs are shown. Mobility degradation in the oxide is divided into two regions, based on the slope: region I is between 70 °C and 130 °C and region II is beyond 130 °C.

Equipped with the information about the transformation with temperature in pentacene thin films and dielectric/pentacene interfacial properties, we have focused the attention on understanding the electrical characteristics of pentacene OFETs with increasing temperature. In Figure 5.6a, b and c, we have compared the extracted saturation mobility, threshold voltage (V_T) and I_{ON}/I_{OFF} ratio respectively for the two types of OFETs, derived from Figure 5.3a and b. The room temperature (at 25 °C) mobility for PS/SiO₂ devices is 0.41 cm²/Vs, which is higher as compared to 0.16 cm²/Vs in oxide OFETs, similar to earlier reports [16]. We found

that on increasing the temperature, the mobility increased slightly in two types of OFETs until 70 °C; this mobility decreased monotonously, relatively more rapidly, on increasing the temperature. It is interesting to note that, in oxide devices, the threshold voltage shifted towards more positive value (decreased) whereas in PS/SiO₂ devices, it shifted in the negative direction (increased). The I_{ON}/I_{OFF} ratio, another figure of merit in OFETs, constantly degraded with the increase in the temperature from 70 °C onward, in both the devices. The decrease in the I_{ON}/I_{OFF} ratio in oxide devices is due to the increase in Off-current (I_{OFF}); however, in PS/SiO₂ OFETs, the decrease in I_{ON} resulted in a reduced I_{ON}/I_{OFF} ratio. The I_{OFF} is defined as the minimum value of current in the measured voltage range. In oxide devices, the I_{OFF} increased with the temperature by almost three orders of magnitude, whereas, the changes were relatively small for PS devices.

First characteristically useful point to be emphasized is that, in oxide devices I_{ON} is almost constant (see Figure 5.3a) although the mobility is decreasing with the increasing temperature. The decrease in the threshold voltage in oxide devices increased the overdrive voltage (V_{GS} - V_T) compensating for the decrease in mobility and effectively retaining the I_{ON} of the devices. The increase in I_{OFF} and the positive shift of the threshold voltage was explained by the increase in carrier injection and activation of trapped carriers with increasing temperature and thermal energy [24]. In PS OFETs, the decrease in I_{ON} and mobility at 110 °C was explained by the degradation of the dielectric-semiconductor interface due to glass transition of PS films at temperature (T_g) of approximately 80 – 90 °C [22, 25].

The observed degradation of mobility for oxide OFETs in Figure 6a initiates around 70 °C. Based on the slope of mobility deterioration, we have divided the degradation mechanism into two regions; region I is between 70 °C and 130 °C and region II is beyond 130 °C. The degradation mechanism in Region I has been attributed to the impact of the temperature on the charge transport and will be discussed later. In region II, the degradation has been attributed to the temperature induced phase transformation of pentacene. As the "thin film phase" transformed to the "bulk phase," different intrinsic attributes started to deform. In the process of the transformation, the crystal structure changed, inducing non-uniform molecular π -overlaps; the morphology changed to a smaller grain size, with a large number of grain boundaries making the over charge transport difficult.

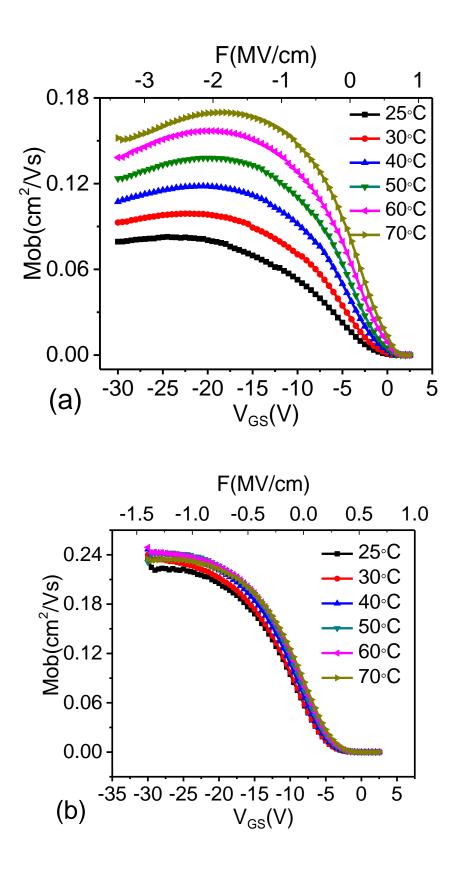


Figure 5.7 Differential mobility extracted from the transfer characteristics in linear regime at $V_{DS} = -2V$ (a) SiO₂ (b) PS/SiO₂ at different temperatures. Electric Field is plotted at the top x-axis.

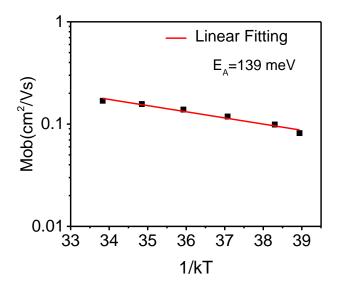


Figure 5.8 Arrhenius fitting of mobility measured on the oxide dielectric with an activation energy of 139 meV

The discussion, thus far, has proven the reliability of pentacene as a semiconductor and identifies 70 °C as a temperature of characteristic transformation. In this small, yet important, range of the temperature we have closely studied the impact of the gate electric field and temperature on the field effect mobility for the two types of OFETs. Figure 5.7a and b plot the differential mobility with the increasing gate voltage at various temperatures for SiO₂ and PS/SiO₂ devices respectively [26]. Since the thickness of the dielectric in the two devices are different, the electric field $(F = (V_{GS} - V_T)/d)$ is plotted on the top axis. In Figure 5.7a, the F is calculated using an average value of V_T measured over different temperatures. Since Figure 5.7a shows differential mobility versus V_{GS} , the peak value of the graph has increased when the temperature increased from 25 °C to 70 °C; the slope of the graph was found to be higher at higher temperatures. At higher temperature, the roll-off of mobility-not prominent at lower temperatures for a typical range of applied V_{GS}—is observed in SiO₂ devices. The mobility increased by a factor of two when the temperature was changed from 25 °C to 70 °C. From these measurements, we calculated the activation energy for the average mobility values within the temperature range and found it to be 139 meV, which is close to the reported values [27]. However, for PS/SiO₂ devices, the mobility was nearly temperature independent within the range of 25 °C to 70 °C, as shown in Figure 5.7b. This was in contrast with the low temperature studies, where mobility was thermally activated on the PS dielectric [28]. Additionally, we did not observe any mobility roll-off for a typical applied V_{GS} range for PS/SiO₂ OFETs.

The increase in mobility and the roll-off of mobility at higher V_{GS} are associated with the properties of SiO₂/Pentacene interfacial defect sites. SiO₂ surface is known to have dangling bonds which acts as trap sites for pentacene devices. The mobility dependence on temperature can be explained by considering the width ($\sigma \approx 95 \text{ meV}$) of the HOMO level for pentacene and the measured activation energy ($E_A \approx 139 \text{ meV}$) of interfacial defect sites for oxide devices. The tail of the HOMO may have overlapped with the shallow trap sites and the charge transport may have been facilitated at higher temperatures due to the thermally activated hopping nature of charge carriers in pentacene. Consequently we can observe enhanced charge carrier mobility within a small increase in temperatures from 25 °C to 70 °C. The roll-off mobility is explained by field-induced degradation due to interfacial defects present at oxide/pentacene interface [29]. With the increasing temperature, carrier injection increases (contact resistance decreases [24]) and as a result, V_T shifts towards a positive voltage. Consequently, the electric field $(F = (V_{GS} - V_T)/d)$ in the channel increases, which increases the concentration of charge carriers at the interface [30]. Due to the presence of a large number traps at the oxide/pentacene interface and the high electric field, increasing carrier density increases the scattering due to interface traps, thereby, decreasing the mobility. The mobility degradation in region I, discussed previously, is due to this roll-off behavior of mobility as pentacene is stable within that temperature range. Above 70 °C, the threshold voltage decrease rapidly (see Figure 5.6b); a corresponding increase in the overdrive voltage (and Electric Field) results in faster mobility degradation. In region II, the net observed mobility degradation is due to the combined effect of roll-off and phase transformation. In PS/SiO₂ devices, the thin layer of non-polar dielectric such as PS passivates the oxide trap sites and the mobility degradation does not occur. The gate voltage independence of mobility in PS/SiO₂ devices can be explained by the filling of all localized states in the accumulation condition and the absence of interface traps [30]. Thus, neither does the increases in temperature have much impact on the mobility, nor is the effect of increased injection is noticeable enough.

5.3.5. Operational stability under Thermal stress

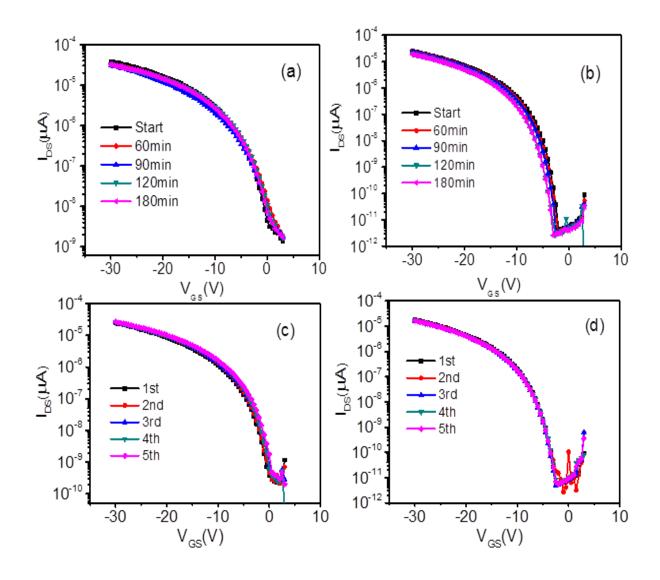


Figure 5.9 Thermal stress (a and b) and fatigue testing (c and d) of OFETs on SiO_2 and PS/ SiO_2 as the dielectric measured at elevated temperature of 70 °C in ambient conditions.

Our analysis thus far has established 70 °C as an optimum temperature of operation of pentacene OFETs on both the dielectrics. Considering the practical requirements discussed in introduction section 70 °C is also an acceptable test limit temperature [4, 5]. The reliability of OFETs at these temperatures cannot be fully established without the thermal stress and fatigue testing. The prolonged stability experiment was performed at a temperature of 70 °C in ambient conditions on both the types of OFETs. Figure 5.9a and b shows the results of thermal stress testing, in which, the devices were continuously heated for 180 minutes and the characteristics were measured at regular intervals. Both, the devices performed reliably with a

less than a five percent variation in the threshold voltage. These results are in concordance with the earlier XPS, XRD and AFM data where the stability of pentacene in a hot air environment was predicted. A temperature of 70 °C creates an environment of warm air around device, thus, reducing the moisture content of the air thus aiding the longevity of the device[31]. Next, the OFETs were systematically characterized for thermal fatigue with repeated heating and cooling cycles. First, the OFETs were measured at 25 °C, then heated to 70 °C for 20 minutes and later cooled back to 25 °C for 10 minutes before being measured again. The transfer characteristics in Figure 5.9c and d were stable for all the five cycles and overlapped meticulously on top of each other, thus, proving the stability of OFETs against any mechanical stress due to heating and cooling cycles.

5.4. Summary

In conclusion, the operational stability of pentacene thin films and pentacene-based OFETs were studied at above-room-temperature range in ambient conditions. The XPS results have proven that the much debated interaction between atmosphere and pentacene does not occur at elevated temperatures. Pentacene based OFETs are operational in ambient conditions at temperatures as high as 190 °C. The charge transport in the above-roomtemperature range is dependent on several factors and mobility can increase, decrease or can be temperature independent depending on the choice of dielectric and the measured temperature range. The inorganic dielectrics offer better temperature stability but the presence of interface traps can severely deteriorates the performance. The thin layer of an organic dielectric like PS can passivate the scattering sites to improve the performance; however, the upper limit of the operating temperature is restricted by the glass transition temperature of organic dielectrics. The crystallinity of the pentacene films is retained till 110 °C and its phase changes around 150 °C. The degradation of OFET characteristics at higher temperature is associated with the polymorphism in pentacene and deterioration of semiconductor-dielectric interface. Based on the electrical, chemical and structural optimization, 70 °C has been identified as the optimum operational temperature for our devices. The device characteristics were found to be stable with thermal stress and fatigue testing. Our work proves the operational stability of OFETs in practical ambient conditions.

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Chapter 6.

Summary and Outlook

In this thesis, we have investigated a series of problems related to the electrical characterization of organic semiconductors. The main aim has been to understand the physics behind electrical characteristics and to use the understanding thus developed to optimize the performance of organic field effect transistors. Organic semiconductors differ from traditional crystalline silicon semiconductors in terms of their intrinsic properties. The electrical characteristics measured in these devices have similar features, but the underlying physics can be very different. Mainly, two types of electrical characterization of organic devices have been focused on in this thesis: capacitance voltage (CV) measurements and current voltage (IV) measurements. The two measurements probe the charge transport in OSC with different points of focus. CV measurements are focused around the charge storing capacity of the devices, whereas, IV are more sensitive to charge conduction.

One of the main findings of this work is the improvement in understanding the capacitance voltage (CV) characteristics of pentacene devices. The CV characteristics of organic semiconductors have visible resemblances to the results measured in doped inorganic semiconductors. Consequently, the explanation of CV behavior has been borrowed from traditional semiconductor physics. Using Mott-Schottky analysis based on the linearity in the

 $1/C^2$ -V curve, the doping density has been extracted. Contrary to inorganic semiconductors, organic semiconductors are used undoped or without any deliberate doping. Subsequently, it led to the idea of "unintentional doping". Due to the atmospheric sensitivity of organic semiconductors (OSC), it is believed that, on exposure to the atmosphere, OSCs can get doped with ambient oxygen. We have thoroughly studied the CV curves and analyzed the validity of Mott-Schottky (MS) analysis for pentacene devices. It is found that the concept of unintentional doping is an analytical artifact due to the inappropriate usage of MS analysis. The CV measurement of pentacene capacitors can be solely understood in terms of the properties of the contact electrodes; unintentional dopants, if any are present, has an inconsequential role in device performance. Our conclusions indicate that, often, an incorrect interpretation of CV results would lead to unphysical values of unintentional doping and has obvious implications in the fundamental understanding of organic device physics, modeling, and characterization, thus, resolving many ambiguities in published work.

Further, Capacitance Voltage measurements were used to analyze the impact of atmospheric exposure on pentacene capacitors. The accumulation characteristics of the devices vary significantly with prolonged atmospheric exposure without a significant change in depletion capacitance. It again proves the invalidity of MS analysis. The degradation in accumulation characteristics is explained by degradation in the injection barrier. An analytical model based on the timing analysis of the capacitance frequency measurement is proposed to extract the degradation in injection barrier. It is found that, on atmospheric exposure, the pentacene gold injection barrier is reduced to 0.51 eV, limiting the number of carriers transporting in the devices. The extracted value is found to be close to the different reported photoelectron spectroscopic studies.

The understanding developed on CV measurements in this thesis can be further extended to study the ohmicity of the contact. Particularly, the process of injection in MIS capacitors with different top metal contacts of varied work functions. The frequency response of the MIS capacitor will depend on the injection barrier at the metal semiconductor interface and the former can be used to extract the barrier. Temperature dependent capacitance frequency measurements will give us the relationship between the process of injection and the temperature. The charge injection is a prerequisite to charge transport. The correspondence between the activation energy of mobility, measured from temperature dependent transistor measurements and cut-off frequency can provide an insight into the factors limiting the charge transport.

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The current voltage experiments were performed on Organic Field Effect Transistors (OFET). OFETs are important devices from both the application perspective and from the perspective of investigating the charge transport. They are extensively studied in this thesis to understand the behavior of mobility under the influence of strain and temperature. The mobility of charge carriers is studied in the top gate bottom contact (TGBC) configuration of OFETs. We have studied the impact of grain size and surface roughness of the active layer on the mobility in top gate n-type C_{60} organic field effect transistors. The morphology was varied by changing the substrate temperature from 100 °C to 200 °C during C_{60} deposition. It was found that for the investigated top gate devices, the mobility does not strictly increase with increasing grain size, which conflicts with the trends reported for bottom gate OFETs. The observation is explained by the fact that the increasing grain size of C_{60} leads to a concurrent increase in the surface roughness, which negatively impacts the charge carrier mobility in the active channel of the OFET. As a result, an optimum of the mobility is reached at 150 °C of the substrate temperature, where grains are already big, comparatively; however, the surface roughness still did not hinder the transport.

The electron transport on the optimized devices at 150 °C of the substrate temperature was further studied to understand the impact of strain on curling. The electron mobility was found to increase (decrease) upon applied compressive (tensile) strain, respectively, when a high-performance, flexible, C_{60} -based organic field-effect transistor (OFET) was subjected to different bending radii. The observed, almost two-fold relative change in the electron mobility was considerably larger than that reported earlier for pentacene-based OFETs. Moreover, the strain dependency of electron mobility in C_{60} films was strongly anisotropic with respect to the strain direction measured relative to the current flow. Analysis within a hopping-transport model for OFET mobility suggests that the observed strain dependency on electron transport is dominated mostly by the change of inter-grain coupling in polycrystalline C_{60} films.

An OFET working in a practical environment has to be able to withstand adverse environmental conditions, including, the ambient exposure and the skewed temperature variations. The different temperature studies, so far, have focused on the low temperature range. Extending the previous studies, we have analyzed the performance and stability of pentacene OFETs in ambient conditions at elevated temperatures. Our material characterization studies prove that the much debated interaction between oxygen and pentacene does not occur even at elevated temperatures. The evolutions of pentacene polymorphs are dependent on the properties of the substrate. The crystallinity of the pentacene films is retained till 110 °C and its phase changes around 150 °C. The electrical characteristics of pentacene based OFETs fabricated on organic and inorganic dielectric is analysed at elevated temperatures in ambient conditions. The organic dielectric leads to a stable performance but their glass transition temperatures can limit the performance of the devices. While inorganic dielectric devices offer better temperature stability, the presence of interface traps at the interface deteriorates the performance. The transistor behaviour in OFET can be seen even at 190 °C. Mobility analysis above the room temperature range reveals a strong dependence on gate field and interface defects. In the presence of traps, thermally activated mobility is observed, whereas, for a trap-free interface, mobility is temperature independent. This study validates the stability and operability of pentacene at an elevated temperature and offers an insight into the device design to increase the optimum temperature of operations.

Appendix A

Capacitance Voltage Measurements

In this thesis, the focus of a major portion of the work has been on the optimization of the capacitance voltage (CV) characteristics of pentacene-based metal-insulatorsemiconductor (MIS) diodes. CV characteristics are difficult to measure as they are very prone to pick up noise from the measurement setup. In this appendix, we have briefly discussed CV measurement techniques and tips to measure CV of organic devices accurately.

The CV measurement in this thesis has been based on the steady state analysis of MIS capacitors. The steady state assumes that the semiconductor parameters of the system are either time-independent or varying sinusoidally in time with time independent amplitudes[1]. The capacitance was measured as a function of the gate bias in a steady state by applying a small signal AC voltage superposed on the DC voltage. The measured capacitance was the differential capacitance $C = \partial Q_T / \partial V_G$, which is dependent on the rate of change of the charge with the applied voltage.

In our experimental setups, the capacitance has been extracted from the imaginary part of the measured complex admittance. There are several models for extracting the capacitance[2]. In this thesis, we have mainly used the model having a parallel combination of capacitance and conductance commonly known as the C_p - G_p model to extract the capacitance. The imaginary part corresponded to the capacitance of the entire device and the conductance was used in calculation of losses through the device. The measured capacitance was equivalent to a series combination of dielectric capacitance and semiconductor capacitance. The proportionate factor of the two components is voltage dependent, as has been shown in Chapter 2.

Capacitance measurement can be tricky as it is prone to noise and measurement errors. For example, the voltage should be applied to the contact with larger surface area in order to minimize the noise. The frequency of the applied AC signal should be determined from the response time of the injected carriers. The applied frequency should be low enough to capture the full response of the carriers; at the same time, caution must be maintained because as the frequency goes down, the noise level increases as well.

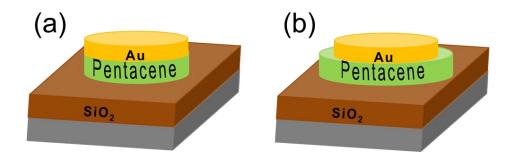


Figure 1 (a) Metal and semiconductor with perfect alignment (b) semiconductor area is larger than metal area.

CV measurement techniques have been established for silicon devices; however, the measurement in organic devices could be different. Organic MIS are mostly inverted in structure, that is, the metal contact is deposited on OSCs (in a silicon device, the top metal contact is deposited on the oxide). Consequently, the area of the deposited OSC is also important, as shown above.

The two structures discussed above lead to two different types of CVs results, as shown in Figure 2. The corresponding frequency response can also vary significantly making the correct interpretation of results difficult. The non-saturation state in Figure 2b is due to the larger area of pentacene compared to the metal contact. Hence, it is important to have alignment between the deposited OSC and the top metal contact. It can be achieved in two ways:

- Aligned metal and semiconductor deposition using the same shadow mask. However, it is often difficult to achieve a perfect alignment in this style of deposition due to differences in the deposition angles of the deposition setups.
- 2. A large-area metal and semiconductor can be deposited and the device can be isolated using pointed objects such as tweezers or needles. This technique results in perfect alignment; however, the area of the different devices will be different and will have to be measured separately.

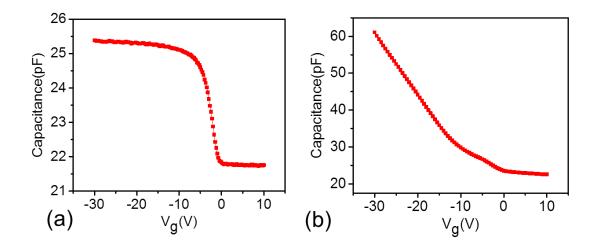


Figure 2. Two CV results obtained for two structures discussed in Figure 1a and Figure 1b are shown, respectively.

CV can be used to extract useful information because it closely follows the process of the injection of charges. However, its results should be carefully analyzed to avoid the misinterpretation. The theory described in Chapter 3 can be useful in extending the CV analysis.

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Appendix B

Sentaurus Simulations

Numerical simulation is a useful technique to model the behavior of semiconductor devices. It provides an easy solution to formulate, debug and verify different physics-based theories. In this thesis, we have used numerical simulations extensively in Chapter 3 to compare the effect of doping with the effect of injection from the contacts, in organic semiconductor.

The Synopsis TCAD tool—Sentaurus Device—has been used for numerical simulations in this work. Terminal currents, voltages and charges have been computed on the basis of a set of user-defined physical device equations that describe carrier distribution and conduction mechanisms. A real semiconductor device, such as an MIS diode, has been represented in the simulator as a "virtual" device whose physical properties have been discretized onto a non-uniform "grid" (or "mesh") of nodes [1].

The device structure used for the simulation was built using box-type architecture, as shown in Figure 1. The different materials have been represented by different color boxes. Conventional materials such as SiO_2 and Aluminum have been defined using the in-built material library. Pentacene has been defined as a general semiconductor and its material

parameters have been defined on the basis of reported literature[2]. Table 1 shows the different material parameters defined for pentacene.

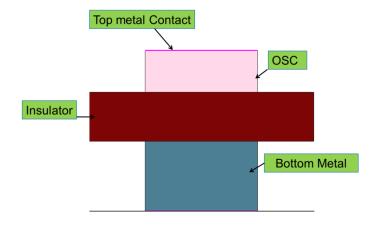


Figure 1 Type device schematic used for simulations of the MIS diode

N _c , N _v	$1 \times 10^{20} \text{ cm}^{-3}$
Dielectric Constant	3.6
Band Gap	2.4 eV
Electron Affinity	2.8 eV
Constant Mobility	$0.1 \text{ cm}^2/\text{Vs}$

Table 1 Material parameter used for pentacene simulations

The physical phenomena in semiconductor devices are very complicated and, depending on applications, are described by partial differential equations of different levels of complexity. The transport model can be selected independently for either of the carriers in the Sentaurus Device. Depending on the device under investigation and the level of modeling accuracy required, transport equations can be selected for simulations. The Capacitance voltage characteristics of the MIS diode have been simulated through self-consistent solutions of the poisson equation for electrostatics, Eq.(1), drift diffusion equations for carrier transport, Eq.(2) and continuity equations, Eq.(3).

$$\frac{d^2 V}{dx^2} = -\frac{n}{\varepsilon} \tag{1}$$

$$J = q\mu nF + qD\frac{dn}{dx}$$
(2)

and,

$$\nabla J = qR_{net} + q\frac{\partial n}{\partial t}$$
(3)

where V is the potential, ε is dielectric constant, n is the carrier concentration, q is the electronic charge, D is the diffusion coefficient and R_{net} is net rate for generation and recombination. Different in-built mobility models are present in Sentaurus; however, for simulations we have used the constant mobility model. The contacts in Sentaurus can be defined as either ohmic or Schottky. The injection barrier in Schottky contacts can be precisely controlled in simulations. The code used for simulations has been given at the end of the appendix.

The Sentaurus Device results generated the measured electrical characteristics along with other physical parameters such as carrier densities, potential, electric field, Fermi level and such others, inside the device. Different measurements of CV characteristics have been shown in Chapter 3. Here, for reference, we have generated the hole density plot inside the device at different biasing voltages, Figure 2.

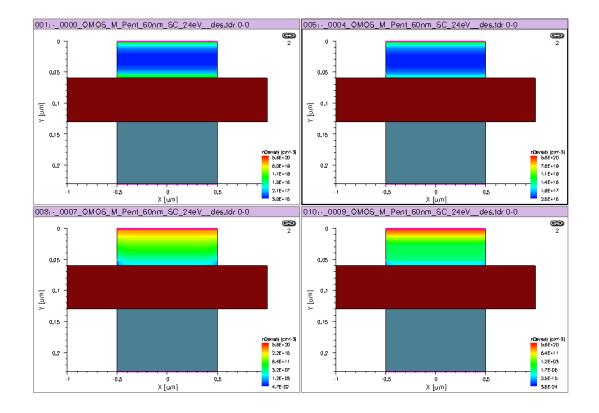


Figure 2 Hole density plotted inside the device at different biasing condition.

Code for Capacitance Voltage simulations of MIS Diode

```
** For MOSCAP only
      ** doing CV with Schottky metal and ohmic metal just change the
barrier line
     Device MOSCAP{
        Electrode {
         { name="Topcontact" Voltage=0.0 }
          { name="Botcontact" Voltage=0.0 Schottky barrier=2.4}
        * Resist=1.89e-9
      }
        File{
                  = "OMOS-Pent msh.tdr"
           Grid
           Plot = "OMOS plot"
          Current = "OMOS current"
          Param = "pentacene.par"
        }
      **Physics (MaterialInterface = "Anysemiconductor/Aluminum") {Schottky}
       Physics {
       AreaFactor = 1.26e5
       *Mobility(DopingDependence Enormal)
       Mobility (ConstantMobility)
       EffectiveIntrinsicDensity(NoBandGapNarrowing) * Bandgap narrowing
should be expllicity stopped
       Recombination (SRH
                     *Band2Band(E2)
                     *Avalanche(CarrierTempDrive)
                    )
      *Fermi
      * to check temperature dependence on CV changing lattice temperature
      * Temperature = 300
      * Thermodynamic
      }
      *** Physics(Electrode="Botcontact"){BarrierLowering}
       }
     Math{
     Method=Blocked SubMethod=Super
     ACMethod=Blocked ACSubMethod=Super
      Extrapolate
       RelErrControl
       Notdamped=50
       Iterations=20
      }
      Plot{
        eDensity hDensity
        eCurrent hCurrent
        ElectricField eEnormal hEnormal
        eQuasiFermi hQuasiFermi
        Potential Doping SpaceCharge
        SRH Auger
        AvalancheGeneration
        eMobility hMobility
        DonorConcentration AcceptorConcentration
       Doping
       eVelocity hVelocity
        ConductionBandEnergy ValenceBandEnergy
      }
      File{
        Output = "n3_des_20.log"
ACExtract = "_AC_"
      }
      System {
```

```
MOSCAP Pent_60nm_00001_24eV_(Topcontact=g Botcontact=b)
       Vsource_pset vg (g 0) { dc = 0 }
        Vsource pset vb ( b 0 ) { dc = 0 }
      }
      Solve{
       * NewCurrentFile="init"
        Coupled(Iterations=100) { Poisson }
        Coupled { Poisson Electron Hole }
       plot (FilePrefix = "At-0V-")
        Quasistationary (
           InitialStep=0.1 Increment=1.3
           MaxStep=0.5 Minstep=1.e-5
           Goal { Parameter=vg.dc Voltage=-10}
        ) { Coupled { Poisson Electron Hole } }
        plot (FilePrefix = "At--10V-")
        NewCurrentFile="CV 60nm 00001 24eV 10Khz "
        Quasistationary (
           InitialStep=0.01 Increment=1.1
           MaxStep=0.01 Minstep=1.e-6
           Goal { Parameter=vg.dc Voltage=10}
        ) { ACCoupled (
             StartFrequency=1e4 EndFrequency=1e4 NumberOfPoints=1 Decade
             Node(g,b) Exclude(vg,vb)
             *ACCompute (Time = (Range = (0 1) Intervals = 20))
           ) { Poisson Electron Hole }
* plot ( FilePrefix="At-midV-" Time= (0.1;0.2;0.25;0.3; 0.4; 0.45;
0.5; 0.55; 0.6; 0.8 ) NoOverwrite )
        }
      }
```

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Appendix C

Hot Wall Expitaxy

Organic semiconductors are deposited mainly through two kinds of processes: 1) Wet processes, such as spin coating, dip coating, drop casting and others, 2) Dry processes such as evaporation. Choosing a deposition process depends on factors such as the cost involved, ease of deposition and quality of films. While the wet processes definitely offer cheaper and easier deposition, the quality of the films is better in dry processes. Hot Wall Epitaxy is a dry deposition technique that has been used in this thesis to deposit high quality polycrystalline C60 films. The experiments were carried out in the Institute of Solid State physics at Johannes Kepler University of Linz, Austria.

The typical dynamics involved in the deposition of a material is physiosorbtion followed by chemisorbtion. In the first step, molecules are adsorbed on the surface, and then, they chemically react with each other to form chemical bonds. However, organic crystals are held together by Van der Waal forces and there is no chemical bonding between the molecules. It is the process of physiosorbtion that primarily determines the quality of the deposited films. The HWE technique allows the deposition under thermodynamic equilibrium conditions—most applicable for organic materials with the Van der Waal binding character [1].

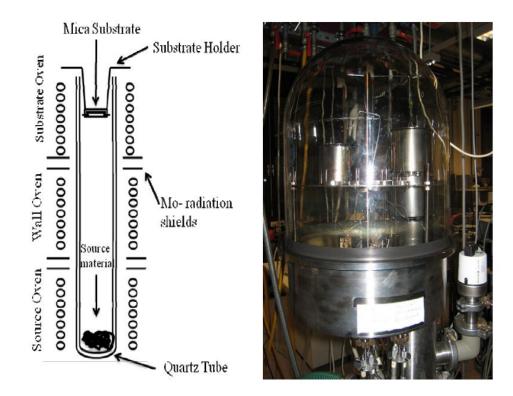


Figure 2 Cross-sectional schematic of a hot wall epitaxy setup along with the photograph of the practical setup.

Figure 1 shows the HWE deposition setup along with the schematic of the setup. HWE is a similar to commonly available evaporation setups and works under high vacuum conditions (~ 10^{-6} mbar). Typically, a hot quartz tube is inserted between the source and the substrate. It limits material loss and offers a clean environment within the deposition chamber. In this manner, a high partial pressure of evaporating material can be maintained in the growth reactor. A cylindrical quartz tube, with the source material at the bottom and the substrate on top of the tube to close it, is placed in a high vacuum chamber between separated and controlled heaters. These heaters represent the three main parts of a typical HWE reactor: the Source heater, Hot-Wall and Substrate heater. The source oven maintains an adequate temperature to evaporate the source material and controls the growth rate. The Hot-Wall region, between the source and substrate guarantees a nearly uniform and isotropic flux of the molecules onto the substrate surface. The substrate oven temperature can influence, to a certain extent, the sticking coefficient and the mobility of the molecules on reaching the substrate surface. Suitable adjustment of these three temperatures enables low supersaturation during growth in the vicinity of the substrate. Hence, it provides effective control over the nucleation stage and, consequently, C_{60} with high crystalline quality can be achieved. High quality C₆₀ films grown using HWE resulted in high mobility n-type transistors[2].

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Appendix D

Fishchuk/Kadashchuk Model

I. I Fishchuk and A. Kadashchuk have developed a charge transport model based on effective medium approximation (EMA) using a Gaussian DOS distribution and the Miller-Abrahams jump rates. The model considers the temperature dependence of the charge carrier mobility in disordered organic solids at high carrier concentrations [1-3]. Their model was intended to stimulate the rationalization of the physics behind the experimentally observed Meyer-Nadal Rule (MNR); they achieved this by using hopping transport in carrier concentration dependents DOS in disordered systems. They successfully demonstrated that the observation of the MNR is a characteristic signature of hopping transport in a random system with variable carrier concentration, irrespective of their polaronic character. We have collaborated with their group in Kiev, Ukraine and used their model to experimentally fit our experimental data.

Within the EMA approach, a disordered organic system is replaced by an effective three-dimensional (3D) manifold of localized sites with an average intersite distance, $a = N^{-1/3}$ where N is the density of the localized states. We have considered an energetically disordered system of localized states characterized by the Density-of-States (DOS) distribution $g(\varepsilon)$ in the framework of the extended Gaussian disorder model (EGDM) [4, 5]

which accounts for the dependence of the mobility on the relative carrier concentration n/N, where *n* is the density of charge carriers. Positional disorder is neglected in this model description.

Let us consider a random 3D hopping transport system with an applied electric field. In general the effective drift hopping mobility μ_e can be obtained as

$$\mu_{e} = ak_{0} \frac{W_{e}^{+} - W_{e}^{-}}{F}$$
(1)

where W_e^+ and W_e^- describe the effective jump rates along-, and opposite- to the electric field direction, respectively, for an arbitrary electric field $\mathbf{F} = \{F, 0, 0\}$. An additional coefficient k_0 emerges in Eq. (1) in order to include the generalized Einstein equation, as recently suggested by Roichman and Tessler [6], relating the mobility and diffusion coefficient at arbitrary carrier concentration. This coefficient is essential, at large carrier concentrations, while in the case of vanishing carrier concentration, $k_0 \rightarrow 1$. Within the average-hopping-times method[7], the effective jump rates W_e^+ and W_e^- can be calculated using the effective transport energy ε_t level as

$$W_{\rm e}^{\pm} = \left\langle \tau_{12}^{\pm} \right\rangle^{-1}, \left\langle \tau_{12}^{\pm} \right\rangle = \frac{\int_{-\infty}^{\varepsilon_{\rm t}} P(\varepsilon) \left\{ W_{12}^{\pm}(\varepsilon_{\rm t},\varepsilon) \right\}^{-1} \mathrm{d}\varepsilon}{\int_{-\infty}^{\varepsilon_{\rm t}} P(\varepsilon) \mathrm{d}\varepsilon}$$
(2)

where W_{12}^+ and W_{21}^- are effective jump rates between two neighboring localized sites along- and opposite- to the electric field direction, respectively. We use a Miller-Abrahamstype jump rate

$$W_{12}^{\pm}(\varepsilon_{t},\varepsilon) = W_{0} \exp\left[-\frac{|\varepsilon_{t} - \varepsilon \mp eaF| + (\varepsilon_{t} - \varepsilon \mp eaF)}{2k_{B}T}\right]$$
(3)

to describe an elementary charge transfer with an applied electric field between sites with energy ε and ε_t being defined in the limit of zero field. Here, $W_0 = v_0 \exp(-2r_t/b)$, where v_0 is the attempt-to-escape frequency, r_t is the jump distance below the effective transport energy ε_t , and *b* is the localization radius of the charged site.

Zero-field charge-carrier drift under thermal equilibrium conditions occurs by carrier hopping transitions between ε and ε_t levels through successive hops downward in energy, toward an empty state ε_1 and then by upward hops to ε_t [7]. Since the downwards hops from the level ε_t occur much faster, the major contribution to the drift time in such paired jumps is determined by the upward hops to the state ε_t . Therefore, configurational averaging of the hopping transitions times in Eq. (2) has to be done over the energy distribution of empty localized states, namely, by using the function

$$P(\varepsilon) = g(\varepsilon) \Big[1 - f(\varepsilon, \varepsilon_F) \Big]$$
(4)

where $f(\varepsilon, \varepsilon_F)$ is given by the Fermi-Dirac statistics

$$f(\varepsilon,\varepsilon_F) = \frac{1}{1 + \exp\left(\frac{\varepsilon - \varepsilon_F}{k_B T}\right)}$$
(5)

The Fermi level ε_F position can be determined from the following transcendental equation for the carrier concentration *n*

$$n = \int_{-\infty}^{\infty} d\varepsilon g(\varepsilon) f(\varepsilon, \varepsilon_F)$$
(6)

The coefficient k_0 (cf. Eq. (1)) in this case can be determined as

$$k_{0} = 1 - \frac{\int_{-\infty}^{\infty} d\varepsilon g(\varepsilon) f^{2}(\varepsilon, \varepsilon_{F})}{\int_{-\infty}^{\infty} d\varepsilon g(\varepsilon) f(\varepsilon, \varepsilon_{F})}$$
(7)

We assume a Gaussian DOS distribution $g(\varepsilon)$, with the width σ as generally accepted to be appropriate for disordered organic media

$$g(\varepsilon) = \frac{N}{\sigma\sqrt{2\pi}} \exp\left[-\frac{1}{2}\left(\frac{\varepsilon}{\sigma}\right)^2\right], -\infty < \varepsilon < \infty$$
(8)

Combining Eq.(1) with Eqs. (2-7), and (8), we can express the effective charge carrier mobility μ_e

$$\mu_{e} = \mu_{0}k_{0}r_{t}^{2} \exp\left(-2\frac{r_{t}}{b}\right) \frac{\left(Y_{e}^{+}\right)^{-1} - \left(Y_{e}^{-}\right)^{-1}}{f}$$
(9)

where

$$Y_{e}^{\pm} = \frac{\int_{-\infty}^{x_{t}} dt \frac{\exp\left\{-\frac{t^{2}}{2} + \frac{1}{2}\left[|x_{t} - t \mp f| + (x_{t} - t \mp f)x\right]\right\}}{1 + \exp\left[-(t - x_{F})x\right]}}{\int_{-\infty}^{x_{t}} dt \frac{\exp\left\{-\frac{t^{2}}{2}\right\}}{1 + \exp\left[-(t - x_{F})x\right]}}$$
(10)

here,

$$Y_{e}^{\pm} = \frac{W_{e}^{\pm}}{W_{0}}, f = \frac{eaF}{\sigma}, x = \frac{\sigma}{k_{B}T}, x_{F} = \frac{\varepsilon_{F}}{\sigma}, x_{t} = \frac{\varepsilon_{t}}{\sigma}, \mu_{0} = \frac{ea^{2}v_{0}}{\sigma}$$
(11)

The effective transport energy ε_t in our method does not depend on the applied electric field *F* and, hence, for a Gaussian DOS distribution can be determined from the following transcendental equation derived for zero-field mobility [4]

$$\frac{1}{\sqrt{2\pi}} \frac{\exp\left(-\frac{1}{2}x_t^2\right)}{1 + \exp\left[-(x_t - x_F)x\right]} \left\{ \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{x_t} dt \frac{\exp\left(-\frac{1}{2}t^2\right)}{1 + \exp\left[-(t - x_F)x\right]} \right\}^{-\frac{4}{3}} = \frac{3}{2} \left(\frac{4\pi}{3B}\right)^{\frac{1}{3}} x \frac{b}{a}$$
(12)

Here, parameter B = 2.7 being determined according to percolation criteria [8]. Factor r_t is calculated by

$$r_{t} = a \left\{ \frac{4\pi}{3B} \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{x_{t}} dt \frac{\exp\left(-\frac{1}{2}t^{2}\right)}{1 + \exp\left[-(t - x_{F})x\right]} \right\}^{-\frac{1}{3}}$$
(13)

Theoretical fitting of charge carrier mobility in chapter 4 has been done using Eqs.(10-13).

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Appendix E

Fabrication and characterization of Organic Field Effect Transistors : Tips and Tricks

During the course of this PhD an important milestone was the successful fabrication of pentacene-based organic field effect transistors. If the devices work, it is all good and, if they do not, every single step needs to be carefully debugged. The OFETs fabricated have a high mobility of $0.5 \text{ cm}^2/\text{Vs}$, negligible hysteresis and highly repeatable device-to-device characteristics. Here, we have listed down the methods and steps found useful while working in the lab:

- 1. Tweezers, petri dishes, container boxes and other accessories used in the fabrication process need to be clean.
- A new p-type or n-type wafer of resistivity < 0.001 ohm-cm was used. Since low temperature resistivity can go up at low temperature measurements.
- 3. Wafers were cleaned using the RCA cleaning process before oxidation.
- 4. An oxide layer of (50 nm to 150 nm) was deposited through the dry oxidation process. Oxide thickness is an important device parameter in controlling the effective channel charge. Smaller thickness results increase the dielectric

capacitance, which in turn, may also increase the gate leakage current—a negative attribute for in FETs.

- 5. The oxide films from thermal oxidation often differ in their hydophilicity. In order to ensure a uniform process at all times, piranaha cleaning of the oxide samples is recommended.
- 6. Piranaha-cleaned oxidized samples tend to have a many dangling bonds on its surface; it is advisable to anneal the samples for at least half an hour at a temperature of 120 °C and above. Caution must be exercised while annealing to ensure that no unwanted dust particles accumulate on the surface of the oxide. It is better to anneal the samples inside a closed set of petri dishes.
- 7. An OSC film can be directly deposited on the cleaned oxide surface; however, for better mobility, a thin layer of organic dielectrics such as PS or PMMA is effective. We have used a solution of 1% of PS (100 mg in 10 ml toluene) as the organic dielectric layer. The solution was spin coated at 2000 rpm for 60 seconds and dried in vacuum. Vacuum drying resulted in a pin-hole-free dielectric layer. The thickness achieved with this above process was 40-50 nm.
- Pentacene films were deposited through vacuum evaporation. The substrate deposition temperature can be varied to alter the film morphology and crystallinity. It is has been observed during several depositions that a deposition rate between 1-5 Å/sec is optimal for high mobility.
- 9. Source drain contacts can be deposited through shadow masks. Shadow masks were prepared in a thin sheet of brass $W/L = 700 \ \mu m / 70 \ \mu m$. (bought from Excel Lasers, MIDC, Andheri, Mumbai). Metal deposition can be complicated. The first 15 nanometers should be deposited at a controlled deposition rate of < 0.5 Å/sec. Once the metal semiconductor contact has been properly established, the deposition rate can be increased.
- 10. The devices have been characterized both inside and outside the glove box. It has been observed that performance does not degrade significantly if good quality OFETs is fabricated. If the fabricated OFETs are not of a good quality, the difference in performance can be huge—depending on the ambient climatic conditions.
- 11. The leakage characteristics are found to be dependent on the coverage of the deposited pentacene. Although organic semiconductors are highly resistive, surface leakage current in OFETs can render the devices unusable. It is advised to pattern the pentacene during deposition.

List of Publications

Journal Publications (Published/Communicated):

- Akash Nigam, Dinesh Kabra, Tarun Garg, Malin Premaratne, and V. Ramgopal Rao, , "Pentacene based Organic Field Effect Transistors at Elevated Temperature in Ambient Conditions", submitted in Organic Electronics
- Akash Nigam, Pradeep Nair, Malin Premaratne, V. Ramgopal Rao, "Role of Injection Barrier in Capacitance Voltage measurements of Organic Devices", IEEE, Electron Device Letters IEEE, 35 (2014) 581-583. (Impact Factor ~ 2.79)
- Akash Nigam, Malin Premaratne, and Pradeep Nair "On the validity of unintentional doping densities extracted using Mott-Schottky analysis for thin film organic devices", Organic Electronics 14 (2013) 2902-2907. (Impact Factor ~ 4)
- Akash Nigam, Günther Schwabegger, Mujeeb Ullah, Rizwan Ahmed, Ivan I. Fishchuk Andrey Kadashchuk, Clemens Simbrunner, Helmut Sitter, Malin Premaratne, and V. Ramgopal Rao "Strain induced anisotropic effect on electron mobility in C60 based organic field effect transistors", Applied Physics Letters 101, 083305 (2012) (Impact Factor ~ 3.8)
- V. Seena, Akash Nigam, Prita Pant, Soumyo Mukherji, and V. Ramgopal Rao. "Organic CantiFET: A Nanomechanical Polymer Cantilever Sensor With Integrated OFET", Journal of Microelectromechanical systems, Vol. 21, No. 2, April 2012 (Impact Factor ~ 2.1)

Conference Publications (Poster/Presentations/Proceedings):

 Akash Nigam, Günther Schwabegger, Rizwan Ahmed, Clemens Simbrunner, Helmut Sitter, Malin Premaratne, and V.Ramgopal Rao, "Impact of Morphology on Charge Carrier Mobility in Top Gate C₆₀ Organic Field Effect Transistors", (Poster + paper) IEEE proceedings of ICEE'2014, held at IISc Bangalore.

- Akash Nigam, Malin Premaratne, and V. Ramgopal Rao, "Capacitance Voltage Measurement As A Technique To Extract Injection Barrier In Organic Devices", poster presentation in ODeFA'14, BARC, Mumbai, India
- Akash Nigam, Pradeep Nair, Malin Premaratne, V. Ramgopal Rao, "Investigating the validity of Unintentional Doping in Pentacene", oral presentation in IU-MRS'2013, IISc, Bangalore, India
- Akash Nigam, Günther Schwabegger, Mujeeb Ullah, Rizwan Ahmed, Ivan I. Fishchuk Andrey Kadashchuk, Clemens Simbrunner, Helmut Sitter, Malin Premaratne, and V. Ramgopal Rao "Anisotropic Strain Effect on Electron Transport in Organic Field Effect Transistors", MRS Fall Meetings'2012, Boston, USA (Talk + Paper).
- Akash Nigam, Ravindra Singh, Sachin Vardham, Sudhir Chandra "A Technique for Fabrication and Packaging of Micro-cantilevers for MEMS", proceedings of ICMEMS' 2009, IIT Madras, India. (Talk + Paper)
- Sachin Vardham, Sudhir Chandra, Anup Vyas, Akash Nigam, Ravindre Singh *"Chemical Detection System Using MEMS Based Microcantilevers*", proceedings of ICMEMS'2009, IIT Madras, India
- Seena V., Nitin Kale, Anukool Rajoriya, Akash Nigam, Soumyo Mukherji and V.Ramgopal Rao "Nano Electro Mechanical systems for Cardiac Diagnostics.", presented at Bangalore Nano conference'2008